國立臺灣科技大學 109 學年度碩士班招生試題

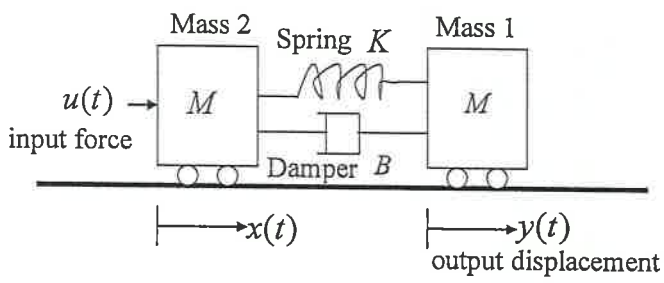
系所組別：電機工程系碩士班丁二組

科　　目：控制系統與數位邏輯

(總分為 100 分)

Problem 1: (15 points) 說明：

Consider the following mechanical translational system where $u(t)$ is the input force, $y(t)$ is the output displacement, and system parameters $M, K, B > 0$;



(a) (10 points) compute the system input-output transfer function $G(s) = \dfrac{Y(s)}{U(s)}$,

(b) (5 points) determine that the system is BIBO (Bounded-Input Bounded-Output) stable or not?

Problem 2: (15 points) 說明：

Consider a negative unity-feedback system with loop transfer function $L(s) = \dfrac{K}{s(s+a)}$, find system parameters K and a such that the maximum overshoot (MO) of the closed-loop system step response is 10.0% and the bandwidth (BW) of the closed-loop system frequency response is 10.0 rad/sec.

Problem 3: (20 points) 說明：

Given a third-order open-loop control system with system input-output transfer function $G(s) = \dfrac{500}{(s+1)(s+5)(s+25)}$;

(a) (10 points) plot the Bode diagram of $G(s)$,

(b) (5 points) compute the gain margin GM,

(c) (5 points) computer the phase margin PM.

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Problem 4 (15 points)

What is the so-called 8-bit timing signal? (5 points) What are the advantages and drawbacks (e.g., the required number of NAND or AND gates, the required function) among three kinds of ring counters to achieve 8-bit timing signal: (i) shift register, (ii) 3-bit counter +3-8 decoder, (iii) Johnson counter. (10 points)

Problem 5 (15 points)

Consider the sequential circuit in Fig. 1, where *A* is the least significant bit. Derive the state table, state diagram, and explain the function that the circuit performs.

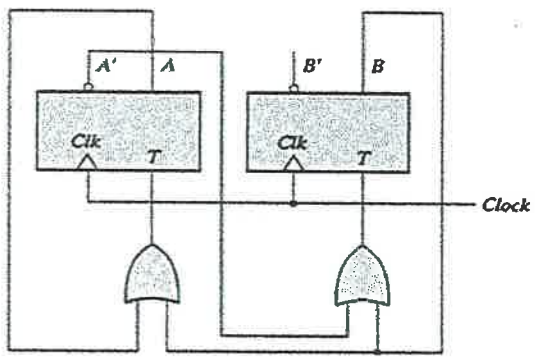

Fig. 1. Sequential circuit 1.

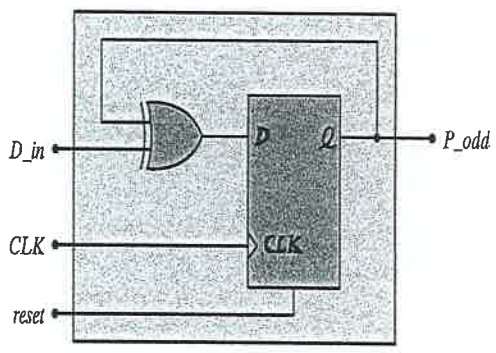

Fig. 2. Sequential circuit 2.

Problem 6 (20 points)

The circuit output of Fig. 2 is asserted if successive samples of the input have an odd number of 1's. These input signals are as follows:

initial #150 **$finish**;
initial fork #1 reset = 1; #7 reset = 0; **join**
initial begin CLK = 0; **forever** #5 CLK = !CLK; **end**
initial begin D_in = 1; **forever** #20 D_in = !D_in; **end**

Write the behavioral and test-bench (using the above inputs) Verilog HDL descriptions of Fig. 2. (13 points) **Plot** the time responses of reset, CLK, D_in and P_odd. (7 points)