1. The circuit of Fig. 1 is designed at a dc emitter current $I_E = 1$ mA and a dc voltage drop across R_B of 1 V. The available power supplies are ±5 V, $\beta = 100$, $V_{BE} = 0.7$ V, and $V_A = 100$ V. If $R_{sig} = 50$ kΩ and $R_L = 1$ kΩ, please find R_{in}, $R_{out}|_{v_{sig}=0}$, and v_o/v_{sig}. (*Note*: In performing the bias design, neglect the Early effect.) (15%)

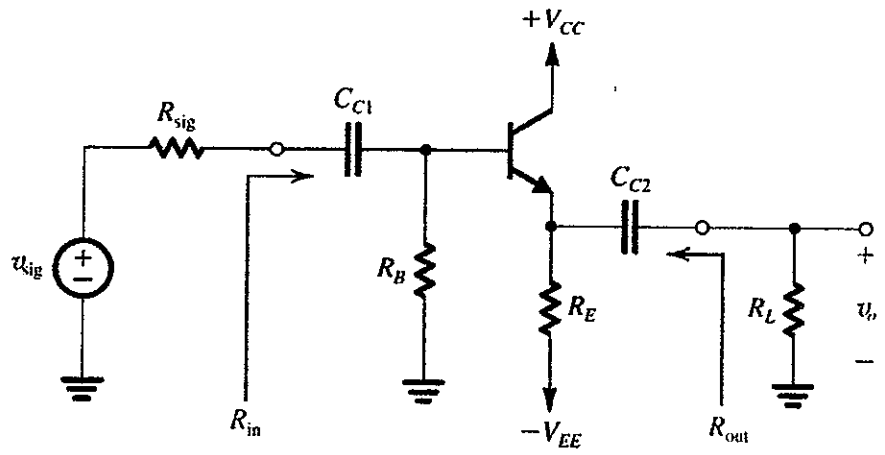

Fig. 1.

2. Assume that the ideal op amp in the circuit in Fig. 2 is operating in its linear region. (a) Calculate the power delivered to the resistor (5%). (b) Repeat (a) with the op amp removed from the circuit, that is, with the resistor connected in the series with the voltage source and the resistor (5%). (c) Find the ratio of the power found in (a) to that found in (b) (5%). (d) Does the insertion of the op amp between the source and the load serve a useful purpose (5%)?

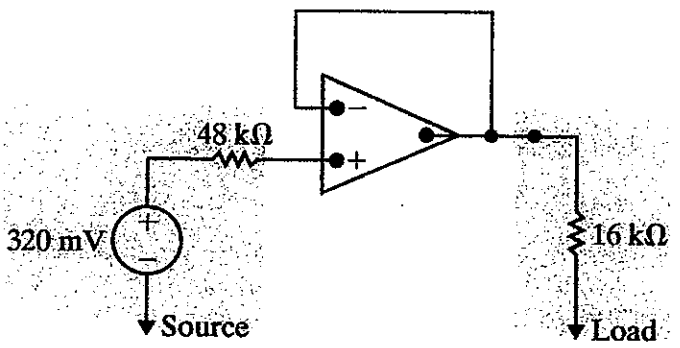

Fig. 2.

3. The switch in the circuit in Fig. 3 has been closed for a long time. At $t = 0$ it is opened. (a) Please write the expression for $i_o(t)$ for $t \geq 0$ (5%). (b) Please write the expression for $v_o(t)$ for $t \geq 0^+$ (5%).

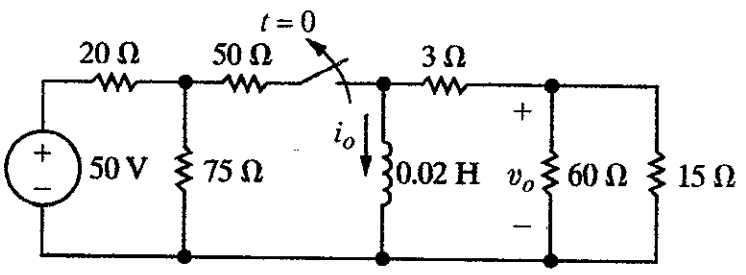

Fig. 3.

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4. The switch in the circuit in Fig. 4 has been in the left position for a long time. At $t = 0$ it moves to the right position and stays there. (a) Please Write the expression for the capacitor voltage, $v(t)$, for $t \geq 0$ (5%). (b) Please Write the expression for the current through the 40 kΩ resistor, $i(t)$, for $t \geq 0^+$ (5%).

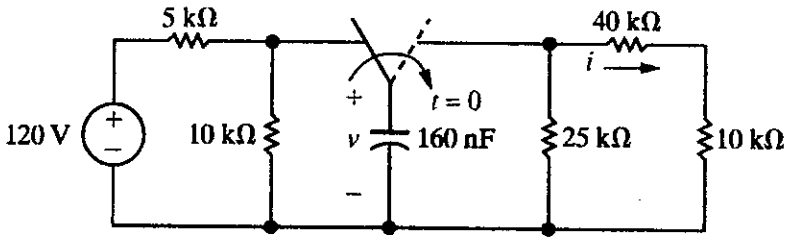

Fig. 4.

5. Design the bias circuit for the CS amplifier of Fig. 5. Assume the MOSFET is specified to have V_t =1 V, k_n = 4 mA/V^2, and V_A = 100 V. Neglecting the Early effect, design for I_D = 0.5 mA, V_S = 3.5 V, and V_D = 6 V using a power-supply V_{DD} = 15 V. (a) Please specify the values of R_S and R_D (4%). (b) If a current of 2 μA is used in the voltage divider, please specify the values of R_{G1} and R_{G2} (8%). (c) Please give the values of the MOSFET parameters g_m and r_o at the bias point (4%). (d) If R_{sig} = 100 kΩ and R_L = 20 kΩ, please use the design obtained from (a), (b), and (c) to determine R_{in}, $R_o|_{v_i=0}$, and the overall voltage gain v_o/v_{sig}. (9%).

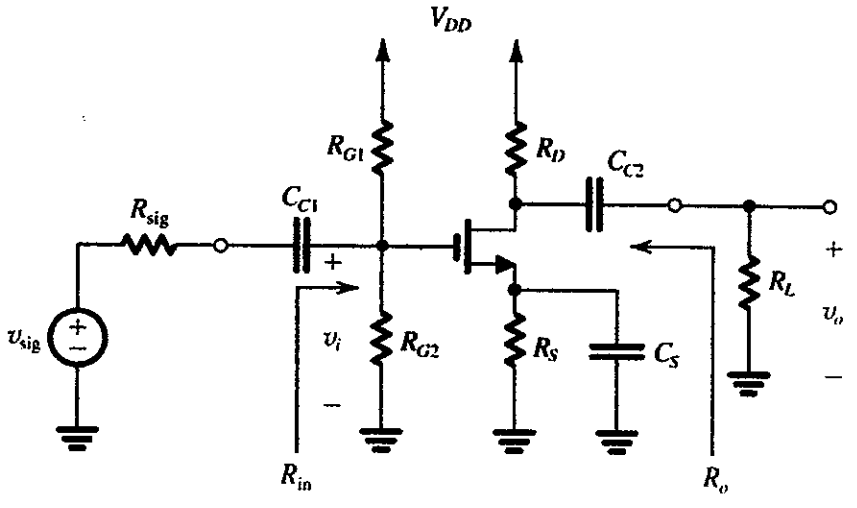

Fig. 5.

6. Please find v_o in the circuit in Fig. 6 (10%). Also please find the power delivered by the dependent source (10%).

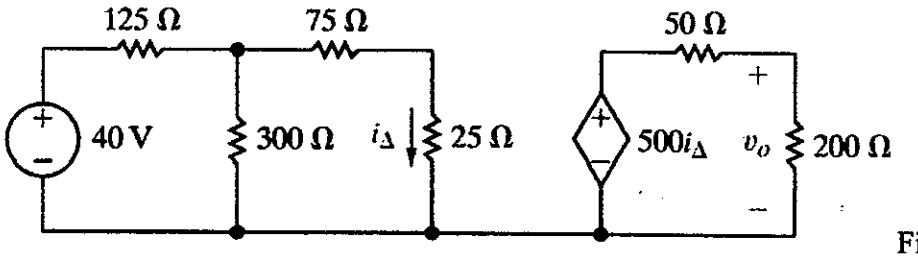

Fig. 6.

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