

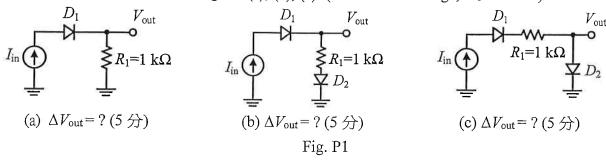
國立雲林科技大學 114 學年度 碩士班招生考試試顯

系所:電子系

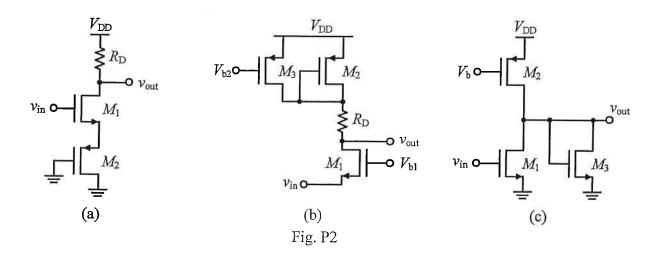
科目:電子學

本試題共 5 題,每題得分如各題中所示,共計 100 分,請依題號作答並將答案寫在答案卷上,違者不予計分。

1. Beginning with $V_{\rm D,on} \approx 800 \, \rm mV$ for each diode, calculate the change in $V_{\rm out}$ if $I_{\rm in}$ changes from 2.0 mA to 2.1 mA in the circuit of Fig. P1 (a), (b), (c). (the thermal voltage, $V_{\rm T} = 26 \, \rm mV$)



- 2. Determine the voltage gain of the stages shown in Fig. P2 (a), (b), (c).
- (a) (5 分) find the voltage gain, v_{out}/v_{in} (Assume $\lambda = 0$).
- (b) (10 分) find the voltage gain, v_{out}/v_{in} (Assume $\lambda \neq 0$).
- (c) (10 %) find the voltage gain, v_{out}/v_{in} (Assume $\lambda \neq 0$).



3. (10 分)Suppose the bipolar transistor in Fig. P3 exhibits the following hypothetical characteristic:

$$I_C = I_S exp \frac{V_{BE}}{2V_T}$$

and no Early effect. Compute the voltage gain for a bias current of 1 mA. (the thermal voltage, $V_T\!=\!26mV$)

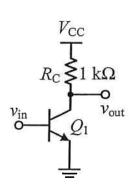


Fig.P3



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4. A closed-loop block diagram is shown in Fig. P4.

- (a) (10 \Re) Derive the transfer function of the loop ($v_{\text{out}} / v_{\text{in}}$).
- (b) (10 %) If A_V is 80 dB and $K_F = 0.5$, what is the total loop gain of this closed loop?

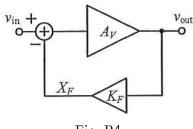


Fig. P4

5. It is known that the common source circuit shown in Fig. P5 has been working in the linear amplification region. (Assume: $V_{DD} = 10 \text{ V}$, $R_D = 10 \text{ k}\Omega$, $R_S = 100 \Omega$, $C_{GS} = 10 \text{ pF}$, $C_{GD} = 2 \text{ pF}$, $C_D = 5 \text{ pF}$, and $gm_1 = 1 \text{ mA/V}$, M_1 without channel length modulation effect)

- (a) (10分) Draw the small signal model of this circuit.
- (b) (10 分) Find the pole frequency at v_{in} .
- (c) (10 分) Find the pole frequency at v_{out} .

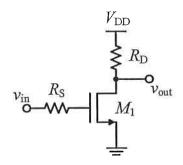


Fig. P5