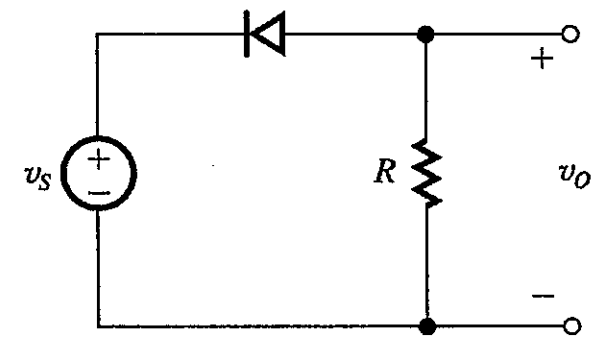
1. (7%) What is harmonic distortion? What causes it?

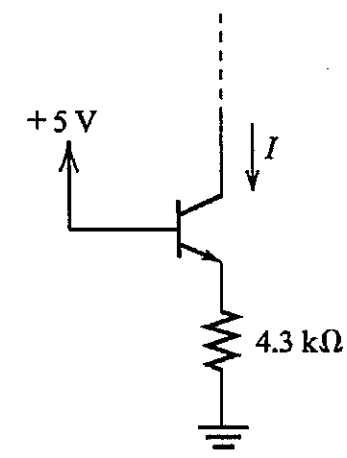
2. (8%) What is the CMRR? For what types of application is it important?

3. (15%) Consider the half-wave rectifier circuit shown on the right. Let v_S be a sinusoid with 10-V peak amplitude, and let $R = 1\ \text{k}\Omega$. Use the constant-voltage-drop diode model with $V_D = 0.7\ \text{V}$.
   (a) Sketch the transfer characteristic.
   (b) Sketch the waveform of v_O.
   (c) Find the average value of v_O.
   (d) Find the peak current in the diode.
   (e) Find the PIV of the diode.



4. (15%) Suppose we have an NMOS transistor that has $g_m = 2\ \text{mS}$ and $r_d = 5\ \text{k}\Omega$ for a Q point of $V_{GSQ} = 2\ \text{V}$, $I_{DQ} = 4\ \text{mA}$, and $V_{DSQ} = 10\ \text{V}$. Sketch the drain characteristics to scale for a small region around the Q point, say, for $v_{GS} = 1.8$, $v_{GS} = 2.0$, $v_{GS} = 2.2\ \text{V}$ and for $9.0 < v_{DS} < 11.0\ \text{V}$.

5. (15%) For the constant-current source circuit shown on the right, find the collector current I and the output resistance. The BJT is specified to have $\beta = 100$, $V_{BE} = 0.7\ \text{V}$, and $V_A = 100\ \text{V}$. If the collector voltage undergoes a change of $10\ \text{V}$ while the BJT remains in the active mode, what is the corresponding change in collector current?



6. (20%) An op amp with bandwidth $f_t = 20\ \text{MHz}$, slew rate $\text{SR} = 10\ \text{V}/\mu\text{s}$, and output saturation $V_{o\max} = 10\ \text{V}$ is used in the design of a noninverting amplifier. The nominal gain of the noninverting amplifier is 10. Assume a sine-wave input with peak amplitude V_i.
   (a) If $V_i = 0.5\ \text{V}$, what is the maximum frequency before the output distorts?
   (b) If $f = 200\ \text{kHz}$, what is the maximum value of V_i before the output distorts?
   (c) If $V_i = 50\ \text{mV}$, what is the useful frequency range of operation?
   (d) If $f = 50\ \text{kHz}$, what is the useful input voltage range?

7. (20%) There is a three-input CMOS NAND gate.
   (a) Draw the circuit diagram of the NAND gate.
   (b) Draw its equivalent circuit (open and closed switches) if all inputs are high.
   (c) Redraw (b) if all inputs are low.

試題隨卷繳回