國立臺灣師範大學 112 學年度碩士班招生考試試題

科目：計算機系統　　適用系所：資訊工程學系

注意：1.本試題共 2 頁，請依序在答案卷上作答，並標明題號，不必抄題。2.答案必須寫在指定作答區內，否則依規定扣分。

1. (20 points) Please answer the following questions about the **process** concept in the O.S. system.

   (a) (10 points) Draw a **Process State Diagram** and explain how a new job/process is transferred from state to state (starting from the first time a job is submitted to its termination).

   (b) (5 points) Use the Process State diagram, and explain how different (i.e., readers and writers) process(es) move from state to state in the **Readers-Writers** problem.

   (c) (5 points) If the problem applies to **no busy wanting**, what will change?

2. (20 points) For the processes shown in the table below.

Process ID	Burst (*ms*)	Arrival Time
P1	10	0
P2	29	1
P3	3	2
P4	7	3
P5	12	4

   Please draw the **Gantt Chart** and compute the **average waiting time**.
   (a) (5 points) **Shortest-Job-First** (SJF)
   (b) (5 points) **First-Come, First Served** (FCFS)
   (c) (5 points) **Round-Robin** (RR) with time quantum = 10 *ms*.
   (d) (5 points) **Multi-level Feedback Queues** with 3 levels and policies as follow:

Level	**Time-slice**	**When dispatched**
1	3 *ms*	
2	5 *ms*	Only when Level 1 is empty
3	FCFS	Only when Level 1 and 2 are empty

3. (10 points) Given the following page reference sequence.
   1 2 7 3 7 0 8 4 0 4 0 4 3 4 3 6 5 0 2 6 1 2 0
   Please use the **LRU strategy** to cache and replace pages. Suppose that we have **3 available frames**, each of which could cache one page. Note that the frames are initially empty.

   (a) (5 points) Show the cached pages in the frames in each step of the page reference sequence.

   (b) (5 points) Calculate the cache miss ratio or page fault ratio, including the initial/compulsory page faults.

4. (10 points) Our favorite program runs in 20 seconds on computer A, which has a 1.5GHz clock rate. We are trying to help a computer designer build a computer B, which will run this program in 9 seconds. The designer has determined that a substantial increase in the clock rate is possible, but this increase will affect the rest of the CPU design, causing computer B to require 1.8 times as many clock cycles as computer A for this program.

   (a) (5 points) What is the CPU clock cycles of A?
   (b) (5 points) What is the CPU clock rate of B?

5. (10 points) Convert the following numbers to decimal numbers.

   (a) (5 points) Unsigned 8bit binary number, 0001111.
   (b) (5 points) Unsigned 16bit hexadecimal number, 04E2.

6. (10 points) Write down the hexadecimal representation of the decimal number 63.25 in the IEEE-754 single precision format.

7. (10 points) Consider a typical five-stage pipelined (IF, ID, EXE, MEM, and WB) RISC processor. Assume there is no forwarding in the pipelined processer. How to add NOP instructions to eliminate hazards in the following sequence of 5 instructions?

   or $r1, $r2, $r3
   or $r2, $r1, $r4
   or $r1, $r1, $r2
   or $r3, $r3, $r4
   or $r4, $r5, $r6

8. (10 points) For a direct-mapped cache design with a 32-bit address, the following bits of the address are used to access the cache.

Tag	Index	Offset
31-10	9-5	4-0

   Starting from power on, the following byte-addressed cache references are sequentially recorded.

   0, 4, 16, 132, 232, 160, 1024, 30, 140, 3100, 180, 2180

   (a) (5 points) How many entries does the cache have?
   (b) (5 points) What is the hit ratio?