· 112CIO

# 國立臺北科技大學 112 學年度碩士班招生考試

系所組別:2300 資訊工程系碩士班

# 第一節 計算機概論 試題

第1頁 共3頁

## 注意事項:

- 1. 本試題共十一題,共100分。
- 2. 不必抄題,作答時請將試題題號及答案依照順序寫在答案卷上。
- 3. 全部答案均須在答案卷之答案欄內作答,否則不予計分。
- 1. Mark by T(=True) or F(=False) each of following statements. You don't need to prove it. (10 pts)
  - (1) For an arbitrary tree with n nodes, there are exactly n-1 edges in that tree. (2 pts)
  - (2) Heapsort is one of the optimal sorting algorithms. (2 pts)
  - (3)  $7n^34^n + n^62^n = O(n^62^n)$ . (2 pts)
  - (4) If edge weights of a connected weighted graph are not all distinct, the graph must have more than one minimum spanning tree. (2 pts)
  - (5) The possible degrees of internal nodes (except the root) in a B -tree of order 7 are 4, 5, 6, and 7. (2 pts)
- 2. Please answer the following question shortly and concisely. You do not need to provide the details. (10 pts)
  - (1) Please write the following infix expression in prefix form: (2 pts)  $((6 \times (5-2)) (8+4)) + ((9/3) \times (1+3))$ .
  - (2) Consider the skip list data structure. Suppose that we use only two levels, i.e., two (sorted) linked lists, for n elements. Each element is in linked list  $S_0$  and some elements are also in the other linked list  $S_1$ . Please draw the skip list structure where the minimized search cost is  $O(\sqrt{n})$ . (2 pts)
  - (3) Consider an 11-entry hash table that uses the hash function,  $h(i) = (2i + 5) \mod 11$ , to hash the keys 34, 22, 2, 88, 23, 72, 11, 39, 20, 16, and 5, with this order. Suppose the collisions are handled by *linear probing*. What's the index of key 72 in the hash table? (2 pts)
  - (4) As the problem in (3), suppose that the collisions are now handled by *double hashing* with the second hash function  $h'(k) = 7 (k \mod 7)$ . What's the index of key 72 in the hash table? (2 pts)
  - (5) Please give the number of binary search trees with n keys. (2 pts)

- 3. Please answer the following questions: (10 pts)
  - (1) A certain integer  $m \le 1000$  has the following modular representations: (2 pts)
    - i.  $m \equiv 1 \pmod{8}$ ;
    - ii.  $m \equiv 2 \pmod{11}$ ; and
    - iii.  $m \equiv 7 \pmod{15}$ .
  - (2) Solve the recurrence relation and present  $b_n$  in close form explicitly:

$$b_n = 3b_{n/2} + \left(\frac{n}{2}\right)^2 - 5\left(\frac{n}{2}\right) + 7,$$

where  $n=2^k$ , for some positive integer k, with the initial condition  $b_1=0$ . (2 pts)

(3) Please find the asymptotic upper bound for

$$T(n) = 3T\left(\frac{n}{2}\right) + n^2 + \log_7 n$$

with T(0) = 1. (2 pts)

- (4) The worst case running time of Randomized Quicksort on *n* elements. (2 pts)
- (5) Give the maximum profit of the continuous-knapsack problem with the following weights( $w_i$ ), profits( $p_i$ ), and knapsack capacity(M): (2 pts)

$$w_1 = 24$$
,  $w_2 = 30$ ,  $w_3 = 27$ ,  $w_4 = 16$ ,  $w_5 = 18$ ;  
 $p_1 = 10$ ,  $p_2 = 12$ ,  $p_3 = 9$ ,  $p_4 = 6$ ,  $p_5 = 8$ ;  
 $M = 80$ .

4. Please find a longest common subsequence of the following two sequences. You need to present the steps for finding the result. (5 pts)

- 5. Please select the correct answer for each one of the following questions. (10 pts)
  - (1) To verify the integrity of a message, we can use a technique. (2 pts)
    - (a) Encryption
    - (b) Digital signature
    - (c) Cryptographic hash function
    - (d) Certificate
  - (2) Which cipher, in the same key size, has a low computational cost? (2 pts)
    - (a) RSA
    - (b) ECC
    - (c) AES
    - (d) ElGamal
  - (3) To prevent the replay attack, we can use a technique. (2 pts)
    - (a) HMAC
    - (b) Authentication
    - (c) Random nonce
    - (d) Encryption

注意: 背面尚有試題

#### 第2頁 共3頁

(4)	To build a safe network for your company, which equipment cannot help you to
	enhance security. (2 pts)
	(a) Firewall
	(b) Rootkit
	(c) DMZ
	(d) Anti-virus software
(5)	The public key system still needs the support of, so that two users can use it
	with confidence. (2 pts)

- (a) Certificate
- (b) Signature
- (c) Password
- (d) None of the above
- 6. For each one of the following questions, please select the correct answer. (15 pts)
  - (1) Please select the correct average wait time under following settings: (3 pts)
    - i. Uses Round-Robin algorithm with time quantum is "10",
    - ii. The order of arrival is P1, P2, P3, P4, and P5,
    - iii. The burst time is P1 = 10, P2 = 9, P3 = 20, P4 = 6, and P5 = 12.
    - (a) 19.4
    - (b) 23.8
    - (c) 17.8
    - (d) None of the above
  - (2) There are three processes: A, B, and C. The burst time of A, B, and C are 3, 6, and 9, respectively. Which arrival order has the least average waiting time when "First-Come-First-Served (FCFS) scheduling is used (3 pts)
    - (a) B, A, C
    - (b) C, B, A
    - (c) A, B, C
  - (3) Which of the following is true? (3 pts)
    - (a) Physical addresses are generated by the CPU during program execution.
    - (b) CPU can directly access data and execute processes from memory and disk.
    - (c) Base and limit register, respectively record the initial memory location of the process and the size of the memory location occupied by the process.
    - (d) About the memory allocation algorithm, the "best fit" means to locate the largest available free portion so that the portion left will be big enough to be useful.
    - (e) None of the above.

- (4) About the deadlock, which of the following is true? (3 pts)
  - (a) If we use the banker's algorithm to control the resource request and allocation, and when we find the system is unsafe, and still grant the resource request, the system will enter the deadlock state.
  - (b) Deadlock can never occur if no process is allowed to hold a resource while requesting another resource.
  - (c) If a deadlock situation arises, the four conditions of mutual exclusion, hold and wait, preemption, and circular wait must hold simultaneously.
  - (d) Deadlock prevention aims to detect and recover the deadlock.
  - (e) None of the above.
- (5) CPU scheduling decisions may take place under the following four conditions:
  - i. When a process switches from the running state to the waiting state
  - ii. When a process switches from the running state to the ready state
  - iii. When a process switches from the waiting state to the ready state
  - iv. When a process terminates

Which of the following is true? (3 pts)

- (a) ii and iii are preemptive
- (b) i and iv are preemptive
- (c) i and ii are non-preemptive
- (d) i and iii are non-preemptive
- 7. Forwarding and routing operate on the network control layer of the OSI model. What are the differences between routing and forwarding? (5 pts)
- 8. Data Link Layer is the second layer in the OSI reference model. What are some of the possible services that a data link layer protocol can offer to the network layer? Which of these data link layer services have corresponding services in IP? In TCP? Please list at least 5 services. (5 pts)
- 9. Suppose an 802.11b station is configured to always reserve the channel with the RTS/CTS sequence. A frame without data is 32 bytes and transmission rate is 11Mbps. Suppose this station suddenly wants to transmit 1,500 bytes of data, and all other stations are idle at this time. What is RTS, CTS, DIFS, SIFS, and ACK? As a function of SIFS (10 usec) and DIFS (50 usec), and ignoring propagation delay and assuming no bit errors, please calculate the time required to transmit the frame and receive the acknowledgment. (10 pts)

### 第3頁 共3頁

- 10. Translate the following C code to MIPS assembly code. (10 pts)
  - (1) Please fill the blanks (a)~(c) with correct statements. (6 pts, each 2pts)

```
C code
01
      int f(int n){
02
           if n \le 1 return 1;
03
           return (2 + f(n-1));
04
MIPS code
      # Function int fun(int n)
02
      fun:
03
              $sp, $sp, -12 #__(a)
04
      sw $ra, 8($sp)
05
      sw $s0, 4($sp)
06
      sw $s1, 0($sp)
07
08
              $s0, $a0
                             # (b)
09
      li $v0. 1
                            # return value for terminal condition
      ble $s0, 1, funExit
10
                            # check terminal condition
11
      addi $a0, $s0, -1
                            # set args for recursive call to fun(n-1)
12
             fun
                            # (c)
13
      move $s1, $v0
                            # store result of fun(n-1) to $s1
      add $v0, $s1, 2
                             # add result of fun(n-1) to $v0
15
      funExit:
16
      lw $ra, 8($sp)
17
     lw $s0, 4($sp)
     lw $s1, 0($sp)
19
      addi $sp, $sp, 12
20
     jr $ra
     ## End of function
```

(2) Assume that the variables **i**, **n** are respectively assigned to registers \$s3 and \$s5, the base address of the array **data** is in register \$s6, and the elements of the array **data** are 4-byte words. Please fill the blanks (d), and (e) with correct statements. (4 pts; each 2pts)

```
C code
01
     while (data[i] == n) {
02
          i = i - 1:
03
MIPS code
     while: sll $t1, $s3, 2
02
           add $t1, $t1, $s6
03
           lw $t0,
                         ($t1)
                                    # (d)
04
           bne $t0, $s5, exit
05
           addi $s3, $s3.
                                     # (e)
06
                 while
     exit: ...
```

- 11. Consider a typical MIPS processor with a 5-stage pipeline datapath as follows. (10 pts)
  - IF: the instruction fetch stage.
  - ID: the instruction decode/register file read stage.
- EX: the execution stage.
- MEM: the memory access stage.
- WB: the write-back stage.
- (1) The following MIPS code is executed on the above processor. (4 pts, each 2pts)

I	code
1	add \$s1, \$t1, \$t2
2	sub \$s1, \$s1, \$s2
3	lw \$s2, 0(\$s1)
4	add \$t1, \$s1, \$s2
5	sub \$t3, \$t2, \$s2
6	sw \$s1, 0(\$t3)
7	or \$t4, \$t2, \$s2
8	add \$t1, \$s2, \$s1

Assume forwarding and stall mechanisms have been designed for the above processor. Please fill in the blanks in the following table when the code sequence runs to the 9 cycle.

Stage	Instruction
IF	
ID	

(2) The following MIPS code is executed on the above processor. (6 pts, each 2pts)

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I	code		
1	add \$s5, \$s3, \$s4		
2	lw \$s2, 16(\$s1)		
3	add \$s0, \$s2, \$s3		
4	sub \$s0, \$s3, \$s4		

- (a) Find all data dependencies in the instruction sequence.
- (b) Find all hazards in the instruction sequence for the processor with and without forwarding.
- (c) Sometimes, even with forwarding, one stage would have to be stalled for a data hazard. The software technique, Reordering Code, would be adopted to avoid the pipeline stalls. Please state if the instruction sequence suffers from a data hazard that cannot be resolved by the forwarding, and list the reordered code.