

長庚大學107學年度研究所碩士班招生考試試題

系所：電子工程學系碩士班

考試科目：電子學

注意：請詳細閱讀下列試題，並請標明題號依試題順序將答案書寫於答案卷上。

本試題共2頁：第 / 頁

- For the circuit in Fig. 1, use superposition to find V_o in terms of the input voltages V_1 and V_2 . Assume an ideal OP Amp. (12%)
For $V_1 = 10 \sin(2\pi \times 60t) - 0.1 \sin(2\pi \times 1000t)$, volts
 $V_2 = 10 \sin(2\pi \times 60t) + 0.1 \sin(2\pi \times 1000t)$, volts
- The differential amplifier in Fig. 2 uses transistor with $\beta = 100$. Evaluate the following: (12%)
(a) The input differential resistance R_{id} .
(b) The overall differential voltage gain V_{od} / V_{sig} (neglect the effect of r_o)

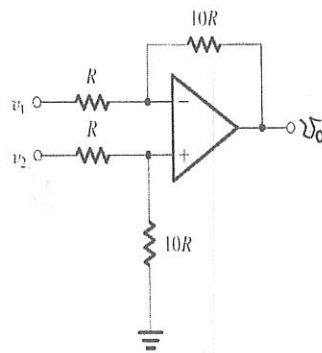


Fig. 1

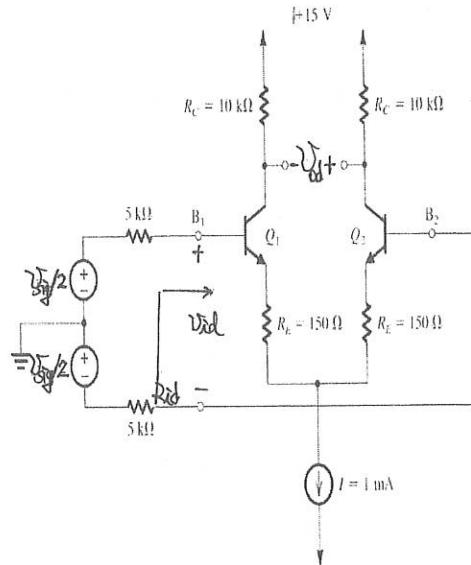


Fig. 2

- The NMOS and PMOS transistors in the circuit of Fig. 3 are matched with $k_n'(W_n/L_n) = k_p'(W_p/L_p) = 1 \text{ mA/V}^2$ and $V_{tn} = -V_{tp} = 1 \text{ V}$. Assume $\lambda = 0$ for both devices, find the drain currents i_{DN} and i_{DP} , and the voltage V_o for $V_i = +2.5 \text{ V}$, and -2.5 V . (15%)
- We want to analyze the circuit of Fig. 4 to determine the small-signal voltage gain V_o/V_s , the input resistance R_{in} , and the output resistance R_{out} . The transistor has $\beta = 100$. (12%)

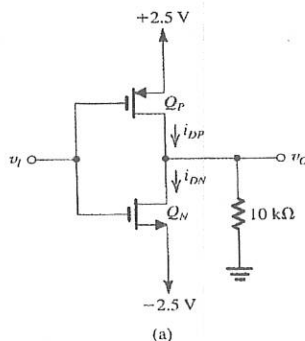


Fig. 3

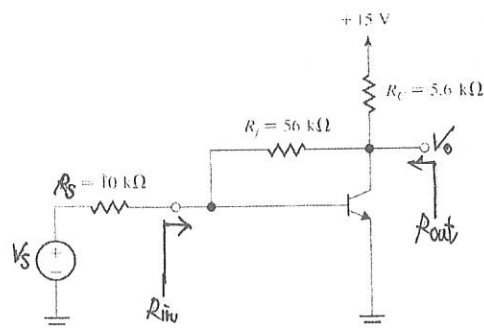


Fig. 4

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5. Please explain the following:
 - (a) Short Channel Effect. (5%)
 - (b) Avalanche breakdown. (5%)
6. Assuming the diodes to be ideal, describe the transfer characteristic of the circuit shown in Fig. 5. (12%)
7. For the circuit in Fig. 6, it is required to determine the value of the voltage V_{BB} that results in the transistor operating (a) in the active mode with $V_{CE}=5V$; (b) at the edge of saturation; (c) deep in saturation with $\beta_{forced}=10$. For simplicity, assume that V_{BE} remains constant at $0.7V$. The transistor β is specified to be 50. (15%)

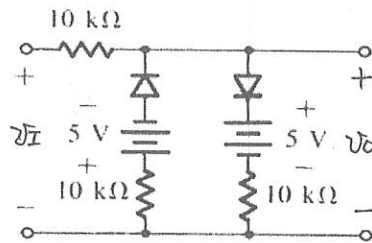


Fig. 5

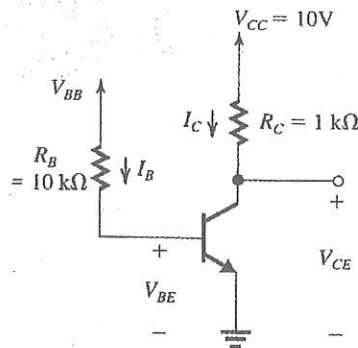


Fig. 6

8. Find I_d (drain current), g_m (transconductance), r_o (output resistance), A_o (open circuit voltage gain), C_{gs} (gate-to-source capacitance), C_{gd} (gate-to-drain capacitance) for an NMOS transistor fabricated in the $0.18\text{-}\mu\text{m}$ CMOS technology specified in the following Table.1. Let $L=0.18\mu\text{m}$, $W=1.8\mu\text{m}$, and $V_{ov}=0.2V$. (12%)

Table.1

Parameter	$0.8\text{ }\mu\text{m}$		$0.5\text{ }\mu\text{m}$		$0.25\text{ }\mu\text{m}$		$0.18\text{ }\mu\text{m}$	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
t_{ox} (nm)	15	15	9	9	6	6	4	4
C_{ox} (fF/ μm^2)	2.3	2.3	3.8	3.8	5.8	5.8	8.6	8.6
μ ($\text{cm}^2/\text{V}\cdot\text{s}$)	550	250	500	180	460	160	450	100
μC_{ox} ($\mu\text{A}/\text{V}^2$)	127	58	190	68	267	93	387	86
V_{th} (V)	0.7	-0.7	0.7	-0.8	0.43	-0.62	0.48	-0.45
V_{DD} (V)	5	5	3.3	3.3	2.5	2.5	1.8	1.8
$ V_A' $ (V/ μm)	25	20	20	10	5	6	5	6
C_{ov} (fF/ μm)	0.2	0.2	0.4	0.4	0.3	0.3	0.37	0.33