考 試 科 目 計算機系統

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資訊科學

考试時

3月19日上午第2年

- COMPUTER ORGANIZATION AND DESIGN

- 1. (6%) Use the following three operations to process 10010011, and choose the correct result.
 - 1.1 (2%) Logical right shift: (A) 10010011 (B) 11100100 (C) 00100100 (D) 01001001 (E) 11001001
 - 1.2 (2%) Arithmetic right shift: (A) 11001001 (B) 01001001 (C) 10010011 (D) 11100100 (E) 00100100
 - 1.3 (2%) Right rotate: (A) 10010011 (B) 11100100 (C) 11001001 (D) 00100100 (E) 01001001
- 2. (3%) Which of the following operation is equivalent to division by 2 in two complement notation, when there is no overflow or underflow? (A) arithmetic right rotate (B) arithmetic right shift (C) arithmetic left shift (D) arithmetic left rotate (E) left rotate
- 3. (3%) Which of the following situation cannot be a binding time? (A) When a program is written (B) When a base register used for addressing is loaded (C) When the instruction containing the address is executed (D) When the program is translated (E) none of the above
- 4. (3%) Addressing modes constitute a very important topic when people discuss alternative designs of CPUs. Common addressing modes include register, immediate, direct, and PC-relative mode, etc. Find a wrong statement from the following choices. (A) Every CPU supports the direct addressing mode. (B) In practice, having immediate, direct, register, and indexed mode is enough for almost all applications. (C) Compilers are in charge of finding the best addressing modes for statements written in high-level languages. (D) When offering a limited number of addressing modes, the architecture must make sure that common applications will be computable. (E) none of the above
- 5. (3%) Assume that you are designing the instruction format for a strange new CPU that will have 16 user-accessible registers. Further assume (1) that all instructions will be encoded in exactly 16 bits and (2) that your boss wants you to include as many instructions that employ register addressing as possible. If each instruction must allow users to use at least two registers, how many different instructions can you get? Which of the following choice is impossible? (A) 64 (B) 128 (C) 256 (D) 512 (E) none of the above
- 6. (3%) Which is not a possible effect of increasing the degree of associativity in the design of cache? (A) decreasing the miss rate
 (B) increasing the hit time (C) requiring more comparators (D) avoiding the needs to bind actual addresses to variable names (E) none of the above
- 7. (8%) Assume a cache of 2K blocks and a 16-bit address. Let α and β, respectively, be the total number of sets and the total number of tag bits for caches that are two-way set associate. Let γ and δ, respectively, be the total number of sets and the total number of tag bits for caches that are fully associative. Compute α/γ and β/δ. You must show the computation process for getting your answers to get credits.
- 8. (8%) In the following C program fragment, which types of hazards might occur in a pipelined machine? Explain your answers.

- (6%) Which of the following architecture/model for multiprocessors systems is most unlikely to adopt techniques of critical sections that are commonly discussed in the course of Operating Systems? Explain your answer. (A) uniform memory access (B) symmetric multiprocessors (C) nonuniform memory access (D) message passing
- 10. (7%) Explain the main difference between the actual meanings represented by the following paired terms.
 - 10.1 (2%) CISC vs. RISC
 - 10.2 (2%) Big endian vs. little endian
 - 10.3 (3%) Programmed I/O vs. DMA

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考試科目計算机年紀 所别 资积科学 考試時間 3月19日上午第二節

- [Basic Concepts] These are true or false problems. If your answer is false please give the true statement with respect to the original false one.
 - (a) (3%) [Virtual Memory] The working-set model is based on the assumption of locality. The most important property of the working set is its size. If we compute the working-set size, WSS_i , for each process in the system, we can then consider $D = \sum WSS_i$, where D is the total demand for frames. Thus process i needs WSS_i frames. If the total demand is greater than the total number of available frames (D > m), thrashing will not occur, because some processes will have enough frames.
 - (b) (3%)[Deadlocks] Given the definition of resource-allocation graph, it can be shown that, if the graph contains no cycles, then no process in the system is deadlocked. If the graph does contain cycle, then a deadlock may exist. This is because if each resource type has exactly one instance, then a cycle does not necessarily imply that a deadlock has occurred.
 - (c) (3%) [Process Definition] A process is more than the program code, which is sometimes known as the text section. It also includes the current activity, as represented by the value of the program counter and the contents of the processor's registers. A process generally does not include the process stack, which contains temporary data (such as method parameters, return addresses, and local variables), and a data section, which contains global variables.
 - (d) (3%) [Page Replacement] The Belady's anomaly is for some page-replacement algorithms, such as FIFO and LRU, the page fault rate may decrease as the number of allocated frames increases. Because we would expect that giving more memory to a process would improve its performance.
 - (e) (3%) [Distributed File Systems] Naming is a mapping between logical and physical objects. There are two naming structures for distributed file systems (DFS): location transparency and location independence. Location transparency indicates that the name of a file does not reveal any hint of the file's physical storage location. While location independence idicates that the name of a file does not need to be changed when the file's physical storage location changes. A location-independence is a stronger property than is location transparency because a location-independent naming scheme is a dynamic mapping.

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[Process Synchronization]

- (a) (5%) Why we have to guard against race condition and synchronize the critical section?
- (b) (5%)A solution to the critical-section problem must satisfy the following three requirements: mutual exclusion, progress, and bounded waiting. Assume the elements of the array boolean flag[2] are initialized false. Please justify whether the following algorithm for the structure of process P_i satisfies these three requirements for the two-process synchronization. Your answer must explicitly justify each condition's satisfaction:

```
do {
    flag[i] = true;
    while (flag[j]);
    critical section
    flag[i]=false;
    remainder section
} while (1);
```

(c) (5%) Please justify whether the following two concurrent serializable transactions T_0 and T_1 schedule S can be transformed into a serial schedule S'.

T_0	T_1
read(A)	
write(A)	
	read(A)
1	write(A)
read(B)	
write(B)	
	read(B)
	write(B)

(Memory Management)

- (a) (5%)An inverted page table has one entry for each real page (or frame) of memory. Design a virtual address scheme in the inverted page table that each entry consists of the virtual address of the page stored in that real memory location, with information about the process that owns that page.
- (b) (5%)Segmentation is a memory-management scheme that supports the user view of memory. Please design a segment table that can map two-dimensional user-defined addresses < segment-number, of f set > into one-dimensional physical addresses.

Mass-Storage Structure] The term fast wide SCSI-II denotes a SCSI bus that operates at a data rate 25 MB per second when it moves a packet of bytes between the host and a device. Suppose that a fast wide SCSI-II disk drive spins at A RPM, has a sector size of B bytes, and holds C sectors per track.

- (a) (5%) Design a formula to estimate the sustained transfer rate of this drive in MB (megabytes) per second.
- (b) (5%) Suppose that the drive has a cylinders, b tracks per cylinder, a head-switch time (from one platter to another) of c milliseconds, and an adjacent-cylinder seek time of d milliseconds. Use this additional information to derive a formula to give an accurate estimate of the sustained transfer rate for a 100 cylinders huge transfer.

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