

考試科目	計算機系統	所別	資訊科學	考試時間	3月18日 星期六	第2節
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## 一. Computer Organization and Design

1. [I/O] (1) Both networks and buses are connected components together. Which of the following are true about them? (6%)
  - (a) Networks and I/O buses are almost always standardized.
  - (b) Shared media networks and multimaster buses need an arbitration scheme.
  - (c) Local area networks and processor-memory buses are almost always synchronous.
  - (d) High-performance networks and buses use similar techniques compared to their lower-performance alternatives: they are wider, send many words per transaction, and have separate address and data lines.(2) In ranking of the three ways of doing I/O, which statements are true? (4%)
  - (a) If we want the lowest latency for an I/O operation to a single I/O device, the order is polling, DMA and interrupt-driven.
  - (b) If we want the lowest impact on processor utilization from a single I/O device, the order is DMA, interrupt-driven and polling.
2. [RAID] What does RAID stand for? (4%) Regarding RAID levels 1,3,4,5, and 6, which one has the highest check disk overhead? (3%) Which one has worst throughput for small writes? (3%)
3. [Memory Hierarchies]
  - (1) Which of the following statements (if any) are generally true? (4%)
    - (a) There is no way to reduce compulsory misses.
    - (b) Fully associative caches have no conflict misses.
    - (c) In reducing misses, associativity is more important than capacity.
  - (2) A new processor can use either a write-through or write-back cache selectable through software. (6%)
    - (a) Assume the processor will run data intensive applications with a large number of load and store operations. Explain which cache write policy should be used.
    - (b) Consider the same question but this time for a safety critical system in which data integrity is more important.
4. [Multiprocessors, Amdahl's law] A program takes  $T_s$  seconds when executed on a single CPU. Now assume that we have  $p$  processors which can be used for parallel processing. (a) If only a fraction  $f$  of the program can be speeded up to take advantage of parallel processing, what is the speedup  $S$ ? (4%) (b) Now assume that the improvement in performance by using  $p$  processor can be formulated as  $p/(1+px)$  for the parallelizable portion, find the value  $p$  that will maximize the overall speedup. (6%)
5. [Floating-point Representation] Consider a shorten version of the IEEE standard floating point format with only 12 bits: one sign bit, 5 bits for the exponent, and 6 bits for the significand.
  - (a) Represent 1.5 and -0.75 with this format. (4%)
  - (b) What is the range of numbers it could represent? (excluding denormalized numbers.) (6%)

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<div>國立政治大學圖書館</div> <p>二. 1. [Basic Concepts] These are true or false problems. If your answer is false please give the true statement with respect to the original false one.</p> <p>(a) (3%) [Context Switch] Switching the CPU to another process requires saving the state of the new process and loading the saved state of the old process. This task is known as a <b>context switch</b>. The <b>context</b> of a process is represented in the Process Control Block (PCB) of a process; it includes the value of the CPU registers, the process state, and memory-management information. When a context switch occurs, the kernel saves the context of the new process in its PCB and loads the saved state context of the old process scheduled to run. Context-switch time is pure overhead, because the system does no useful work while switching.</p> <p>(b) (3%)[Semaphore] A semaphore <i>S</i> is an integer variable that, apart from initialization, is accessed only through two standard atomic operations: <b>wait</b> and <b>signal</b>. Although under the classical definition of semaphores with busy waiting the semaphore value is never negative, we may still have negative semaphore values in the implementation. If the semaphore value is negative, its magnitude is the number of processes waiting on that semaphore. A binary semaphore is a semaphore with an integer value that can range only between 0 and 1 while a counting semaphore its integer value can range over an unrestricted domain. In fact, a counting semaphore can be implemented using binary semaphores.</p> <p>(c) (3%) [Dynamic Loading] To obtain better memory-space utilization, we can use <b>dynamic loading</b>. With dynamic loading, a routine is not loaded until it is called. All routines are kept on disk in a relocatable load format. The main program is loaded into memory and is executed. The advantage of dynamic loading is that unused routine is never loaded. Dynamic loading does not require special support from the operating system. It is the responsibility of the users to design their programs to take advantage of such a method. Operating systems may help the programmer, however, by providing library routines to implement dynamic loading.</p> <p>(d) (3%) [Network File Systems (NFS)] NFS views a set of interconnected workstations as a set of independent machines with independent file systems. The goal is to allow some degree of sharing among these file systems in a transparent manner. Sharing is based on a client-server relationship. Two separate protocols are specified for these services: a mount protocol and the NFS protocol. The mount protocol provides a set of RPCs for remote file operations. The procedures support the following operations: searching for a file within a directory; reading a set of directory entries; manipulating links and directories; accessing file attributed; reading and writing files.</p> <p>(e) (3%) [Protection] The main differences between capability lists and access lists for the implementation of access matrix are: each row in the access matrix can be implemented as an access list for one object while the capability list associates each column with its domain so a capability list for a domain is a list of objects together with the operations allowed on those objects.</p>						
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<div>國立政治大學圖書館</div> <div>2. [Process Synchronization]</div> <div>(a) (6%) Demonstrate what are the appropriate conditions on using semaphores, conditional critical regions, and monitors to solve the process synchronization problem?</div> <div>(b) (4%) Describe the Dining Philosophers Problem?</div> <div>(c) (5%) How do we model Dining Philosophers Problem as a process synchronization problem (Note: you can use either semaphore or monitor primitives to explain your design philosophy but you do not have to write their complete source code)?</div> <div>3. [Memory Management]</div> <div>(a) Consider a two-level page-table scheme, in which the outer page table itself is also paged with the page table stored in memory:</div> <div><div>i. (2%)If a memory reference takes 90 nanoseconds, how long does a paged memory reference take?</div><div>ii. (3%)If we add TLBs, and 95 percent of all page-table references are found in the TLBs, what is the effective memory reference time? (Assume that finding a page-table entry in the TLBs take 9 nanoseconds, if the entry is there.</div></div> <div>(b) (5%)Consider a demand-paging system with a paging disk that has an average access and transfer time of 15 milliseconds. Addresses are translated through a two-level hierarchical paging systems with a page table in main memory, with an access time of 2 microsecond per memory access. Thus, each memory reference through the page table takes two accesses. To improve this time, we have added an associative memory that reduces access time to one memory reference, if the page-table entry is in the associative memory. Assume that 85 percent of the accesses are in the associative memory, and that, of the remaining, 30 percent (or 4.5 percent of the total) cause page faults. What is the effective memory access time?</div> <div>4. [Protection]</div> <div>(a) (5%) What is the <b>confinement problem</b>? Why we said this problem is in general unsolvable?</div> <div>(b) (5%) In a ring-protection system, level 0 has the greatest access to objects, and level <math>n</math> (greater than zero) has fewer access rights. The access rights of a program at a particular level in the ring structure are considered as a set of capabilities. What is the relationship between the capabilities of a domain at level <math>j</math> and a domain at level <math>i</math> to an object (for <math>j &gt; i</math>)?</div> <div><div>備考</div><div>試題隨卷繳交</div></div> <div><div>命題委員：</div><div>66</div><div>(簽章)</div></div>						

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