國立中山大學102學年度碩士暨碩士專班招生考試試題

科目名稱：數位電路【電機系碩士班丙組選考、己組】　　題號：431007

※本科目依簡章規定「可以」使用計算機（廠牌、功能不拘）　　

[Problem 1] (20%) Short answer questions:

(a) Give one example to show that "the simplest expression of a Boolean function may not be unique". (4%)

(b) Give a general structure of a sequential circuit and use this structure to explain the differences of a sequential circuit from a combinational circuit (4%)

(c) What is a Mealy finite state machine? (2%) Give one design example of a Mealy finite state machine. Note that you need to give the function of this design and its state diagram. (5%)

(d) Give some waveforms to explain the meaning of the setup time and the hold time of a D flip-flop. (5%)

[Problem 2] (18%) Design a synchronously resettable positive edge-triggered finite state machine that has a one-bit input d and two outputs x and y. x should be 1 if d has been 0 for at least two cycles (not necessarily consecutively). y should be 1 if d has been 0 for at least three consecutive cycles. For example, the input sequence d=0101100011010 results in the output x=0011111111111 and the output y=0000000100000.

(a) Give Verilog/VHDL codes of a synchronously resettable positive edge-triggered flip-flop. (3%)

(b) Draw the state transition diagram and define each state clearly. (5%)

(c) Write RTL Verilog/VHDL codes to implement the finite state machine you designed in (b). (10%)

[Problem 3] (15%) 2-4-2-1 is a useful 4-bit binary code to represent decimal digits, as listed in Table 1. Design a combinational circuit F that can check if the decimal input encoded by 2-4-2-1 is a prime number, i.e., a positive integer that is greater than 1 and can be exactly divided by only 1 and itself. That is, the output F of the circuit equals 1 if and only if the decimal input is a prime number. You need to show the truth table of this circuit and design the two-level NAND-NAND network using the minimum number of logic gates and literals. Please note that the input code words (w, x, y, z) and their complements can be used directly as fan-in in the final logic diagram, and the unused input code words can be used as don't care conditions for logic simplification.

Table 1

Decimal digit	2-4-2-1 code
0	0000
1	0001
2	0010
3	0011
4	0100
5	1011
6	1100
7	1101
8	1110
9	1111

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[Problem 4] (15%) Design an asynchronously resettable positive edge-triggered counter with the following repeated binary sequence: 0, 3, 1, 4, 7, 5, 2, 6. Note that the counter must have the parallel-load capability, i.e., the content of the counter can be arbitrarily specified via the circuit inputs.

(a) Draw the state transition diagram and define each state clearly. (5%)

(b) Write RTL Verilog/VHDL codes to implement the counter. (10%)

[Problem 5] (20%) Implement the following Boolean function

$F(w, x, y, z) = xy + w'xy' + w'x'z' + wx'y'z' + wx'yz.$

(a) by using only NOR and inverter gates. (5%)

(b) by using only AND and inverter gates. (5%)

(c) by using the simplest sum-of-products form (5%)

(d) by drawing the logic diagram using a multiplexer (5%)

Please note that for (a), (b) and (c) you only need to show the final Boolean function and how you derive the function.

[Problem 6] (12%) Memory related questions.

(a) What is RAM? (2%)

(b) What is ROM? (2%)

(c) Explain in detail how to write and read a memory, respectively. (3%)

(d) Give some waveforms to explain the meaning of the access time and the cycle time of a memory. (5%)