

國立高雄第一科技大學 97 學年度 碩士班 招生考試 試題紙

系所別：電子與資訊工程研究所

組別：不分組

考科代碼：2301

考科：電子學

注意事項：

- 1、本科目可使用本校提供之電子計算器。
- 2、請於答案卷上規定之範圍作答，違者該題不予計分。

1. Sketch a Widlar current source and explain the operation. (10 %)
2. Discuss an advantage of BiCMOS circuit. (10 %)
3. Explain the phase and gain margins. (10 %)
4. Sketch an active filter and indicate the -3dB point. (10 %)
5. Describe and explain the opration of a Wien-bridge oscillator. (10 %)
6. Describe and explain the opration of an astable multivibrator. (10 %)
7. Describe and explain the opration of a Differential Ampilifier. (10 %)
8. For the circuit in Figure 1, the transistor parameters are: $K_{n1} = K_{n2} = 4 \text{ mA/V}^2$, $V_{TN1} = V_{TN2} = 2 \text{ V}$, and $\lambda_1 = \lambda_2 = 0$. Determine (a) I_{DQ1} , I_{DQ2} , V_{DSQ1} , and V_{DSQ2} . (b) g_{m1} and g_{m2} . (c) the overall small-signal voltage gain $A_v = v_o / v_i$. (3%, 3%, 4%)

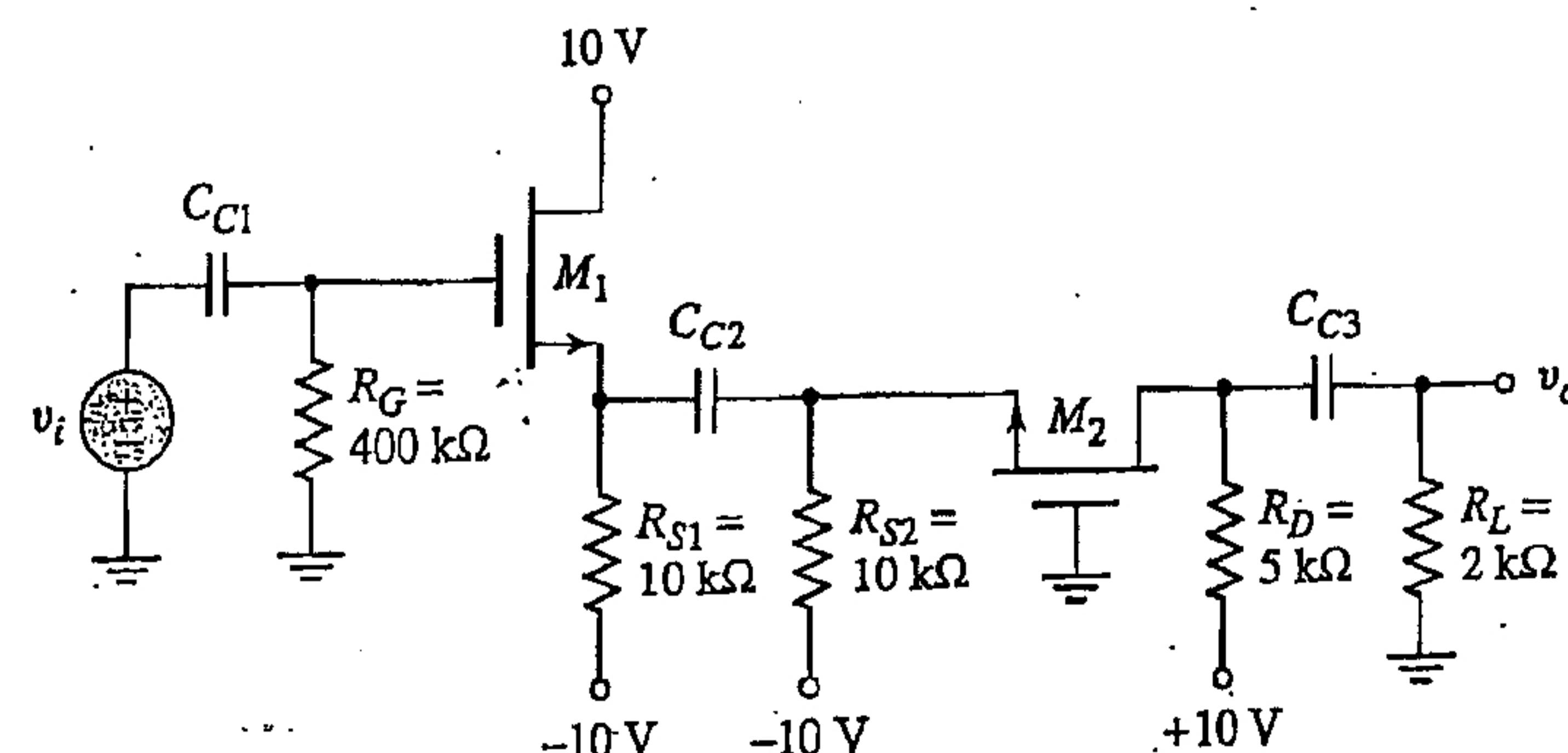


Figure 1 第 1 頁，合計 2 頁【尚有試題】

9. Design a common-emitter circuit whose output is capacitively coupled to a load resistor $R_L = 10\text{ k}\Omega$. The minimum small-signal voltage gain is to be $|A_v| = 50$. The circuit is to be biased at $\pm 5\text{V}$ and each voltage source can supply a maximum of 0.5 mA. The parameters of the available transistors are $\beta = 120$ and $V_A = \infty$. (10%)

10. Consider the circuit shown in Figure 2 where $v_s = 4 \sin \omega t$ (mV). Assume $\beta = 80$. (a) Determine $v_o(t)$ and $i_o(t)$. (b) What are the small-signal voltage and current gains? (10%)

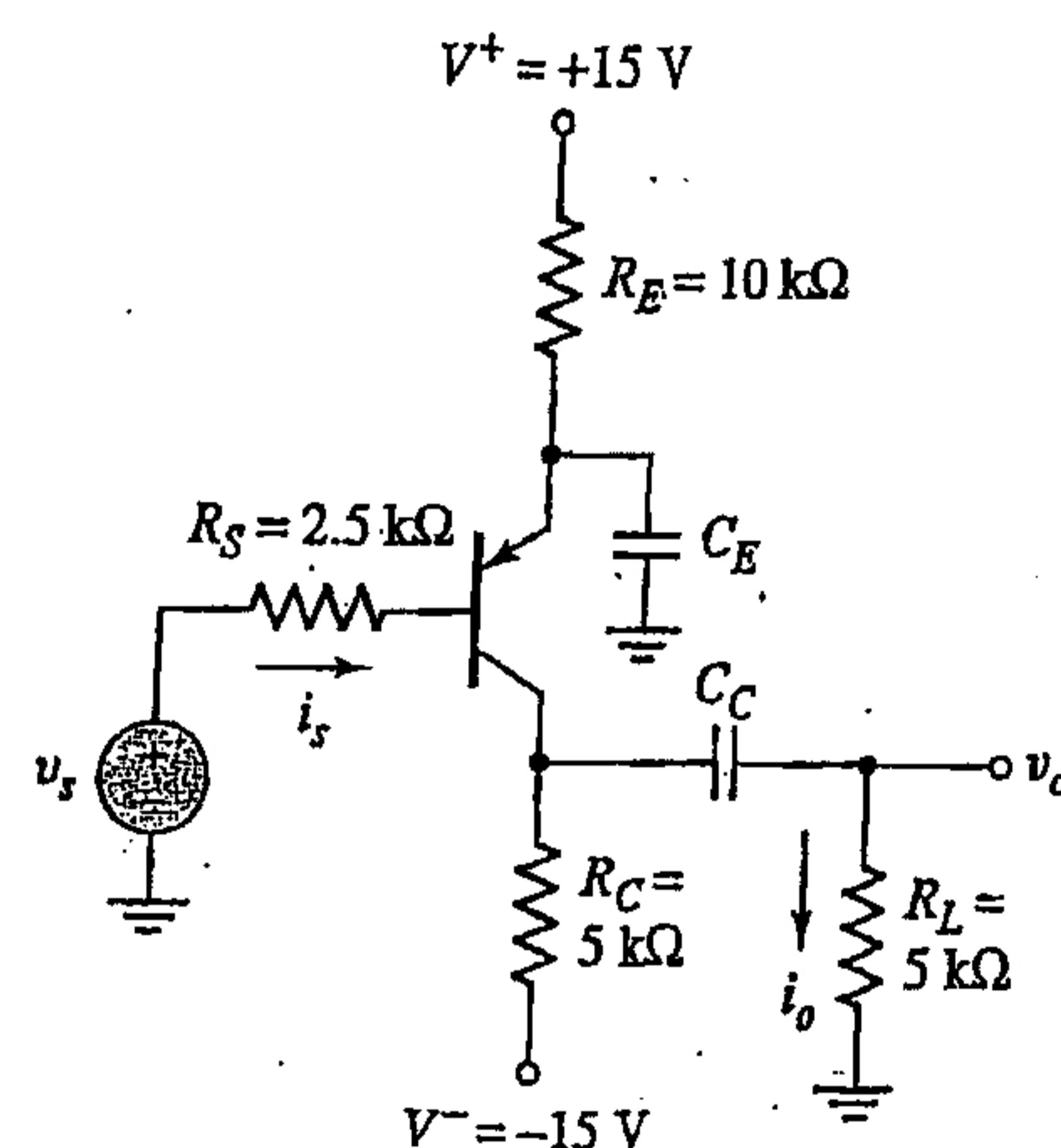


Figure 2