國立高雄應用科技大學
九十七學年度碩士班招生考試
電子工程系（丙組）

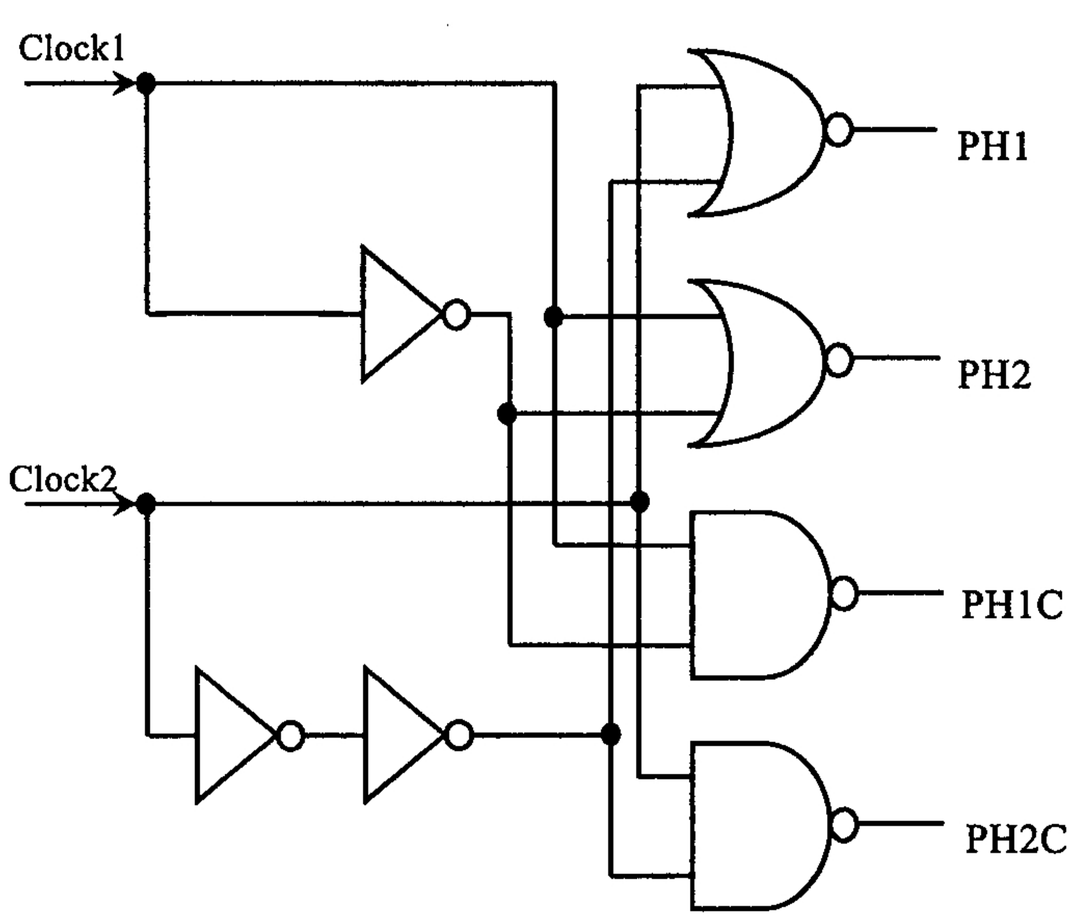
准考證號碼□□□□□□□□□□　（考生必須填寫）

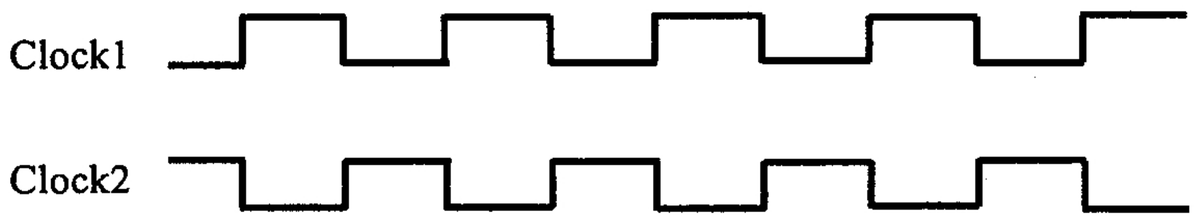
計算機結構

試題　共 3 頁，第 1 頁

注意：a. 本試題共 5 題，每題 20 分，共 100 分。
b. 作答時不必抄題，各試題答案必須依題號順序寫在試卷指定的答案欄。
c. 考生作答前請詳閱答案卷之考生注意事項。

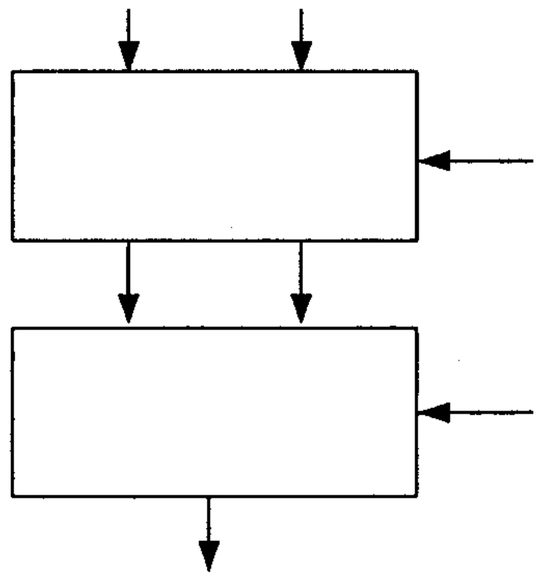
1. (20%) For the following phase-clock generator with two input of clock1 and clock2, draw the waveforms of PH1, PH2, PH1C and PH2C if the delay through NOT, NOR and NAND gates can be ignored.





2. (20%) Consider the combinatorial circuits for adder and multiplier.
   (a) A half-full adder (HA) can perform addition of two bits but a full adder (FA) can perform addition of three bits. Draw a full adder using half-full adders and some logic gates, where the block circuit of a half-full adder is shown below.

   (b) If a 3×3 Wallace-tree multiplier using a 5-bit carry-save adder and 6-bit parallel adder (i.e., ripple carry adder) is constructed as follows, where a multiplication of (111) × (110) is shown below.



x = 1 1 1
y = 1 1 0
0 0 0 ← *PP0*
1 1 1 ← *PP1*
1 1 1 ← *PP2*
1 0 1 0 1 0 ← *Final Product*

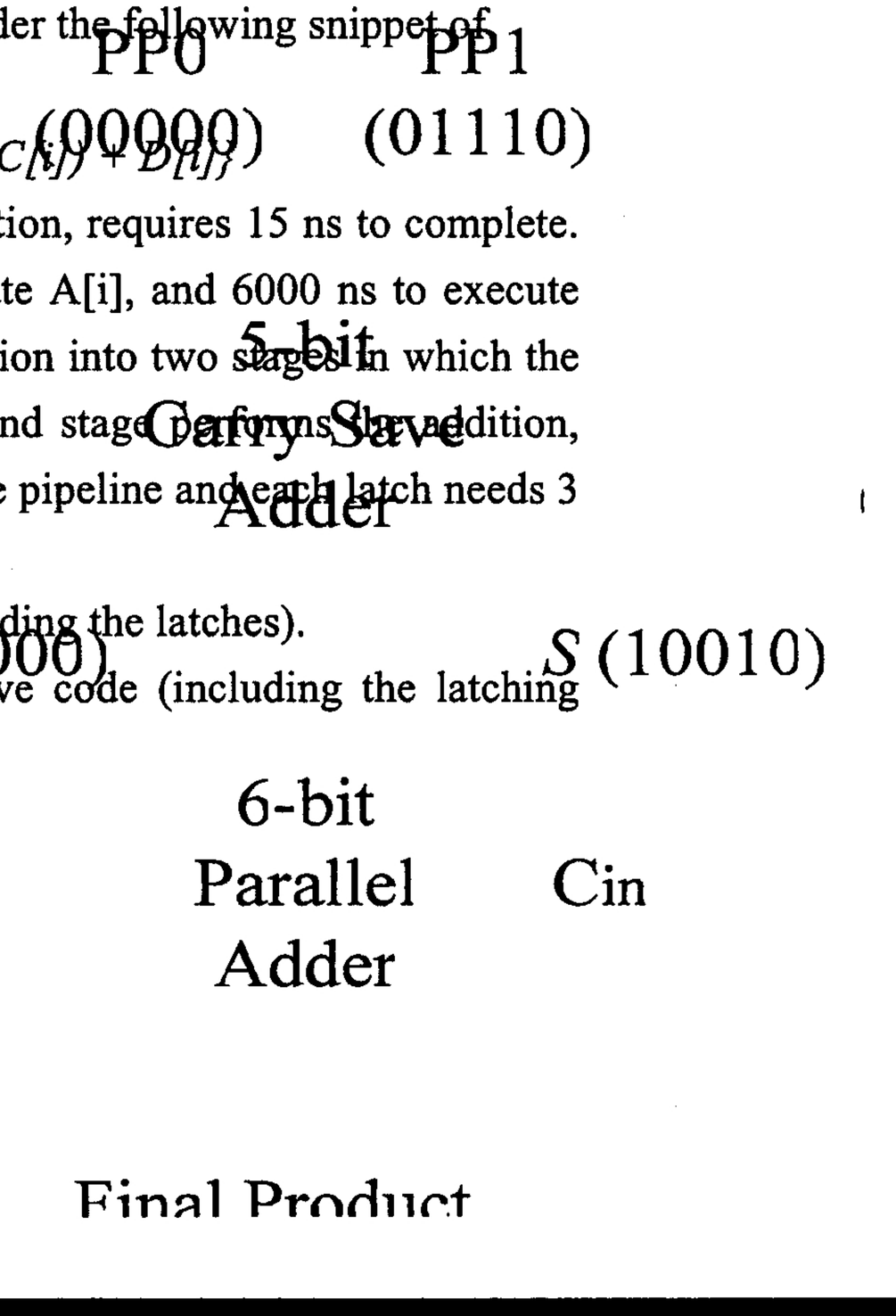
According to the above construction, construct a 4×4 Wallace-tree multiplier using one 7-bit and one 8-bit carry-save adders and one 9-bit parallel adder for a multiplication of (1011) × (1110).

3. (20%) For the pipeline in computer arithmetic, consider the following snippet of code:

*For I = 1 TO 200 DO {A[i] = (B[i]*C[i]) + D[i]}*

Assume that each operation, multiplication and addition, requires 15 ns to complete. A non-pipelined uniprocessor takes 30 ns to calculate A[i], and 6000 ns to execute the code. A pipelined unit could break this computation into two stages in which the first stage performs the multiplication and the second stage performs the addition, where the latches store the output of each stage in the pipeline and each latch needs 3 ns to load data.

   (a) Draw the above two-stage pipeline scheme (including the latches).
   (b) Calculate the time required to execute the above code (including the latching time).



4. (20%) Consider some instructions for the 8085 microprocessor in the following table.
   (a) What is the function provided by the following program fragment?
   (b) After executing the following program fragment if using n = 5, find

   A = ? B = ? Z (zero-flag) = ? xx = ?

Instruction	**Operation**
NOP	No operation
LDA addr	A = M[addr]
STA addr	M[addr] = A
MOV r1, r2	r1 = r2
ADD r	A = A + r
SUB r	A = A - r
INR r	r = r + 1
DCR r	r = r - 1
ORA r	A = A ∨ r
XRA r	A = A ⊕ r
JUMP addr	GOTO addr
JNZ addr	IF (Z=0) THEN GOTO addr (where Z is zero-flag)

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        LDA n
        ADD A
        MOV B, A
L1 :    XRA A
        ADD B
        DCR B
        JNZ L1
        STA xx
```

5. (20%) (a) Assume a microprocessor has 20-bit address bus and 16-bit data bus. The memory utilization involves 64K bytes for I/O device, 64K bytes for EPROM device, and others for SRAM. How many SRAM devices of size 64Kx8 are required in such a microprocessor?
   (b) For four storage devices in a computer: cache memory, register, main memory, and hard disk, compare the speed of these four storage devices.
   (c) For operations in stack, write 4 operations of PUSH and/or POP for executing the exchange of registers A and B contents.
   (d) Consider a multiplication using ROM table, what is the size of the ROM for realizing the multiplication of two 4-bit operands ?