國立雲林科技大學
97學年度碩士班入學招生考試試題

乙、丁組

系所：電機系
科目：電子學

1. In the circuit in Fig.1 with transistor parameters $\beta = 180$ and $V_A = \infty$, design the bias resistors $R_1$ and $R_2$ to achieve maximum symmetrical swing in the output voltage and to maintain a bias-stable circuit. The total instantaneous C-E voltage is to remain in the range $0.5 \le v_{CE} \le 4.5\,\text{V}$ and the total instantaneous collector current is to be $i_C \ge 025\,\text{mA}$. $(R_1 // R_2 = 1.81k\Omega)$ (25%)

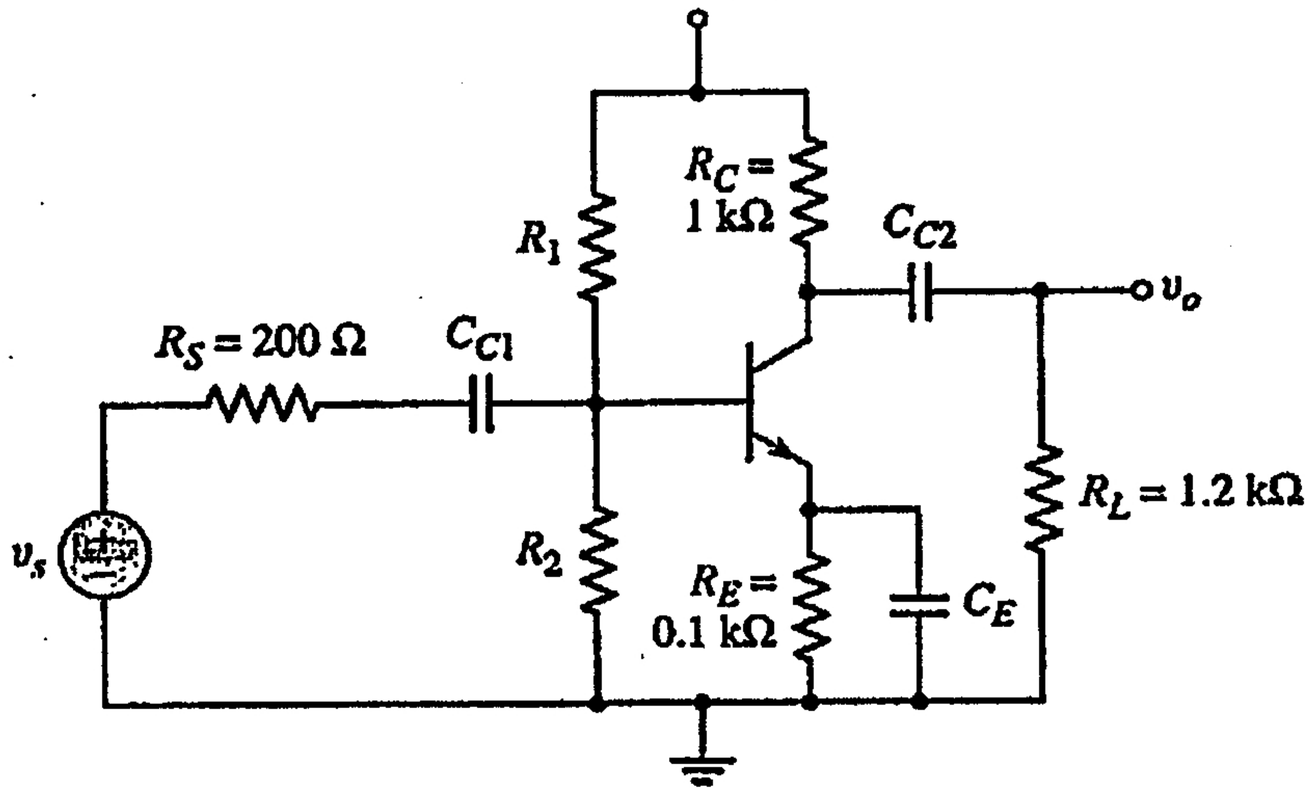


Fig.1

2. For the circuit shown in Fig.2, the transistor parameters are: $I_{DSS} = 6mA$, $|V_p| = 2V$, and $\lambda = 0$. (a) Calculate the quiescent drain current and source-to-drain voltage of Q1 (10%) (b) Derive the expression of the overall small-signal voltage gain. (15%)

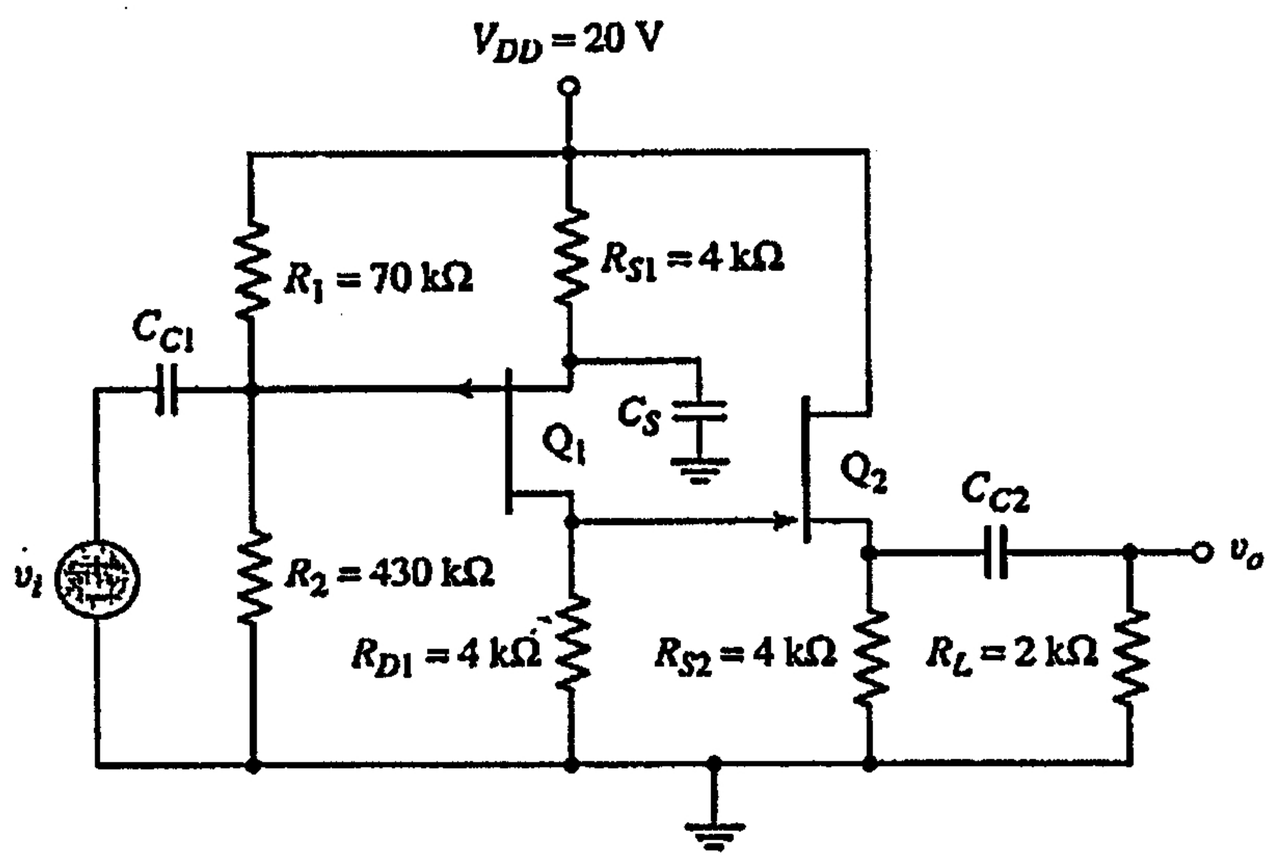


Fig.2

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3. For the MOSFET circuit shown in Fig. 3, the transistor parameters are : $\frac{1}{2}\mu_n C_{ox}\frac{W}{L}=1\text{mA/V}^2$, $V_{TN}=1\text{V}$, $\lambda=0$, $C_{gs}=2\text{pF}$, $C_{gd}=0.5\text{pF}$.

(a) Calculate $I_D$, $g_m$. (5%)

(b) Draw the simplified high-frequency equivalent circuit. (5%)

(c) Find the midband voltage gain. (5%)

(d) Calculate the equivalent Miller Capacitance. (5%)

(e) Determine the upper 3dB frequency for the small-signal voltage gain. (5%)

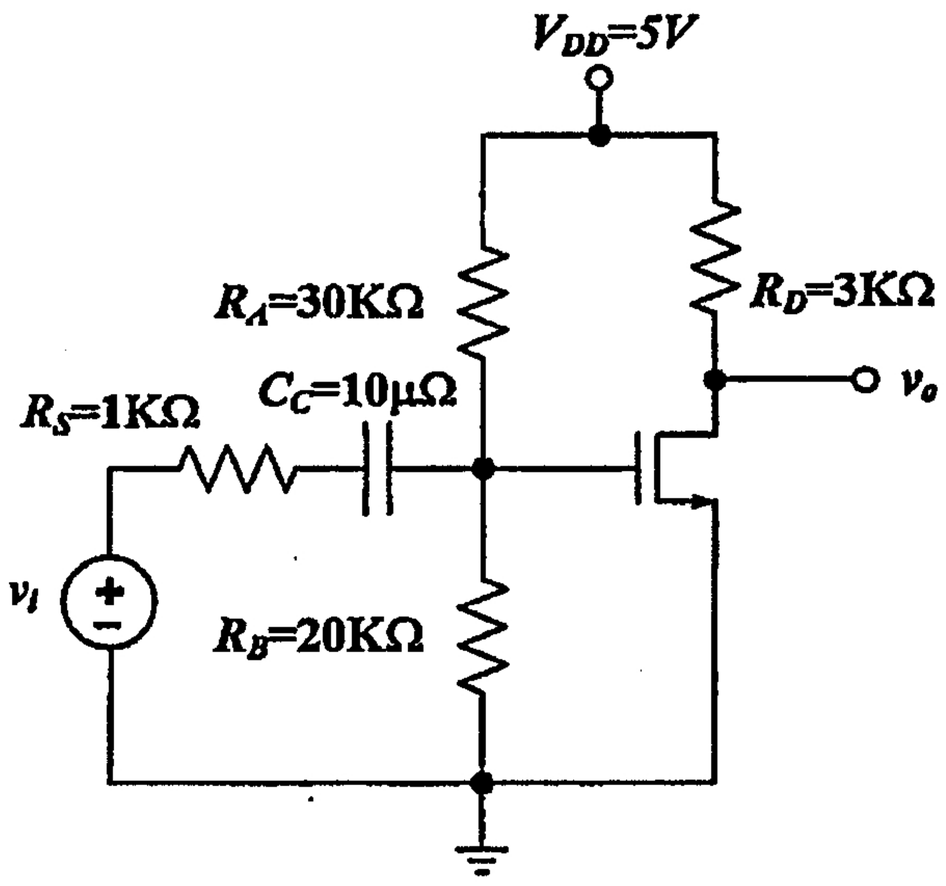


Figure 3

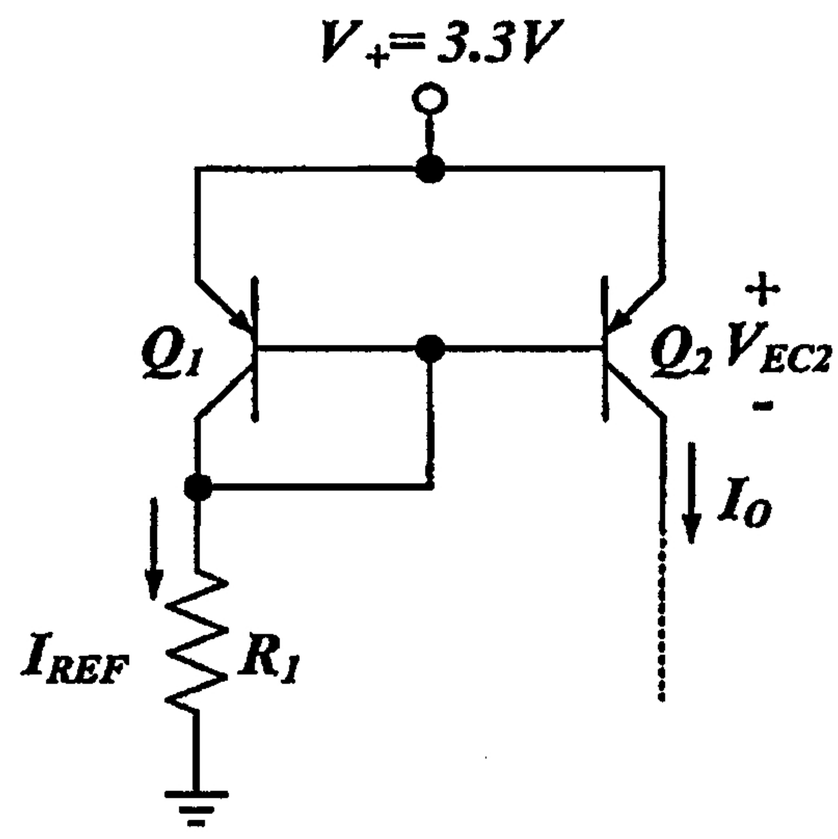


Figure 4

4. Figure 4 shows a basic two-transistor pnp current source. The transistor parameters are : $\beta=50$, $V_{EB}(\text{on})=0.6\text{V}$, and $V_A=50\text{V}$. The transistor value of $R_1$ is designed at 9KΩ. Determine $I_O$ for (a) $V_{EC2}=0.6\text{V}$, (b) $V_{EC2}=2\text{V}$. (10%)

5. Consider a four pole feedback loop system with a loop gain given by

$$T(f)=\frac{\beta(10^4)}{\left(1+j\frac{f}{10^6}\right)\left(1+j\frac{f}{10^7}\right)\left(1+j\frac{f}{10^8}\right)\left(1+j\frac{f}{10^9}\right)}$$

Determine the value of $\beta$ and the frequency that produces a phase margin of 45 degrees. (15%)