# 國立高雄應用科技大學 <br> 100 學年度研究所碩士班招生考試 

## 光電與通訊工程研究所碩士班

准考證號碼 $\square \square \square \square \square \square \square \square$（考生必須填寫）

## 電子學

試題 共 4 頁第 1 頁

注意：a．本試題共 5 题，每題 20 分，共 100 分。
b．作答時不必抄題，但必須書寫計算過程否則不予計分。
c．考生作答前請詳閉答案卷之考生注意事項，各試題答案必須依题號順序寫在試卷指定的答案欄；寫錯位置不予計分。

1．For the circuit in Fig．1，calculate the values：（a）dc gain（ $V_{o} / V_{s}$ ），（b）3－dB frequency， （c）frequency at which the gain becomes 0 dB （i．e．unity）for the case $R_{s}=20 \mathrm{k} \Omega$ ， $R_{i}=100 \mathrm{k} \Omega, R_{0}=200 \Omega, R_{L}=1 \mathrm{k} \Omega, C_{i}=60 \mathrm{pF}$ ，and $\mu=144 \mathrm{~V} / \mathrm{V}$ ．（20\％）


Fig． 1

2．For the circuit shown in Fig．2，express $v_{o}$ as a function of $v_{1}$ and $v_{2}$ ．（a）What is the input resistance seen by $v_{1}$ alone？（b）What is the input resistance seen by $v_{2}$ alone？ （c）By a source connected between the two input terminals？（d）By a source connected to both input terminals simultaneously？（20\％）


Fig． 2

3．For the circuit shown in Fig．3，both diodes are identical，conducting 10 mA at 0.7 V and 100 mA at 0.8 V ．Find the value of $R$ for which $V=80 \mathrm{~V}$ ．（20\％）


Fig． 3

4．Fig． 4 shows a discrete common－source MOSFET amplifier utilizing the drain－to－gate feedback biasing arrangement．The input signal $v_{i}$ is coupled to the gate via a large capacitor，and the output signal at the drain is coupled to the load resistance $R_{L}$ via another large capacitor．The transistor has $V_{t}=1.5 \mathrm{~V}, k_{n}^{\prime}(W / L)=0.25 \mathrm{~mA} / \mathrm{V}^{2}$ ，and $V_{A}=50 \mathrm{~V}$ ．Assume the coupling capacitor to be sufficiently large so as to act as short circuits at the signal frequencies of interest．Find：（a）small－signal voltage gain，（b）input resistance，（c）the maximum allowable input signal peak．（20\％）


Fig． 4

5．For the emitter－follower circuit shown in Fig．5，the BJT used is specified to have $\beta$ values in the range of 40 to 200．For the two extreme values of $\beta, \beta=40$ and $\beta=200$ ， find：（a）$I_{E}, V_{E}$ ，and $V_{B}$ ，（b）the input resistance $R_{i n}$ ，（c）the voltage gain $v_{o} / v_{s i g}$ ． （20\％）


Fig． 5

