中原大學 102 學年度 **碩士班** 入學考試

102/3/2 10:00 ~ 11:30 電子工程學系晶片與系統組

誠實是我們珍視的美德，
我們喜愛「拒絕作弊，堅守正直」的你！

科目：數位電路 （共 2 頁第 1 頁）

□可使用計算機，惟僅限不具可程式及多重記憶者 ☑不可使用計算機

1. [10%] Perform addition on the given numbers using **2's complement** to representation. Use a word length of 6 bits (including sign) and indicate if an overflow occurs.
   (a) 16 + (-9) (b) (-12) + (-22)

2. [20%] Consider the Boolean function f(A,B,C,D)= Σm(1, 3, 4, 9) which has don't care conditions d(A, B, C, D)= Σ(5, 6, 11)
   (a) Use a variable Karnaugh map with the method of map-entered variables to simplify the Boolean function in a **minimum** (1) **sum-of-products (SOP)** and (2) **product-of-sums (SOP)** expressions, respectively.
   (b) Plot the circuit using only (1) **NAND** gates (2) **NOR** gates

3. [15%] (a) Write a **truth table** for a **half adder**. Use **AND, OR, and NOT** gates to **implement** the half adder.
   (b) Use **half adders** and some AND, OR, or NOT gates to form a **1-bit full adder**.

4. [15%] Answer the following questions.
   (a) What is different between a **latch** and a **flip-flop**?
   (b) What is different between a **combinational logic circuit** and a **sequential circuit**?
   (c) What is different between a **Mealy machine** and a **Moore machine**?
   (d) What is the **setup time** of a flip-flop?
   (e) What is the **hold time** of a flip-flop?

5. [15%] A sequential circuit has two *D* flip-flops A and *B*, two inputs x and y, and one output z. It is specified by the following next-state and output equations:

   $A(t+1) = A'y' + Bx$

   $B(t+1) = Ax + B'y$

   $z = A + B$

   (a) Draw the **logic diagram** of the circuit.
   (b) List the **state table** for the sequential circuit.
   (c) Draw the corresponding **state diagram**.

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6. [25%] Design a 3-bit counter that is initially reset to the 000 state. The counting sequence is 000 -> 101 -> 111 -> 110 -> 010 -> 001 -> 000.
   (a) **Plot** the state diagram of this counter.
   (b) Use **J-K** flip-flop to design this counter. List the next-state tables and derive the corresponding input equations.
   (c) Use **Verilog** or **VHDL** language to describe this counter circuit.