元智大學 102 學年度研究所 **碩士班** 招生試題卷

系(所)別：電機工程學系碩士班　組別：電子工程組　科目：電子學　用紙第 1 頁共 2 頁

●不可使用電子計算機

1. (20%) Given an *n*-channel MOSFET with $k'_n = 100\ \mu A/V^2$, $V_{tn} = 0.7$ V, and $W/L = 10$, find the drain current i_D in the following cases:
   (a) $v_{GS} = 3$ V and $v_{DS} = 1$ V (10%)
   (b) $v_{GS} = 2$ V and $v_{DS} = 1.3$ V (10%)

2. (10%) Please sketch the pull-down network (PDN) of a MOS logic circuit that realizes the function $Y = \overline{A} + \overline{B}(\overline{C} + \overline{D})$.

3. (10%) Please describe the static power dissipation and dynamic power dissipation for a complementary metal-oxide-semiconductor (CMOS) logic-circuit family.

4. (55%)A two stage amplifier with feedback network is shown in Fig. 1. For the following circuit, assume $\lambda = 0$ and transconductances of transistors M_1 and M_2 are g_{m1} and g_{m2}, respectively. Meanwhile, $R_1+R_2 >> R_{D2}$
   (a) Please indicate which transistor will be suffered from body effect. (5%)
   (b) What components construct the first stage of the amplifier? (5%)
   (c) What components construct the second stage? (5%)
   (d) What components construct the feedback network? (5%)
   (e) What kind of feedback topology is it? (5%)
   (f) Please derive the open-loop input impedance? (5%)
   (g) Please derive the open-loop output impedance? (5%)
   (h) Please derive the open-loop voltage gain? (5%)
   (i) Please derive the closed-loop voltage gain? (5%)
   (j) Please derive the closed-loop input impedance? (5%)
   (k) Please derive the closed-loop output impedance? (5%)

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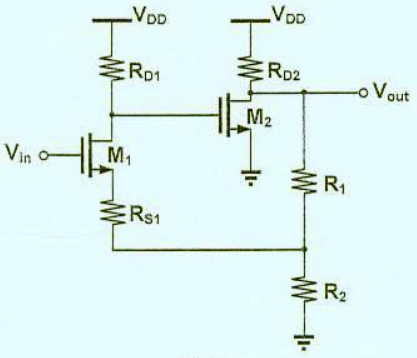

Fig. 1

(2) (5%) Please explain the Miller's Theorem.