元智大學 102 學年度研究所 碩士班 招生試題卷

系(所)別：通訊工程學系碩士班　組別：微波組　科目：電子學　用紙第 / 頁共 2 頁

●不可使用電子計算機

1. Assume a constant-voltage mode (D_{on} = 0.7 V) for the diodes. (a) Plot the output voltage waveform of a full-wave rectifier as shown in Fig.1 with a sine wave input signal . 7% (b) Explain how this circuit works. 7%　14%

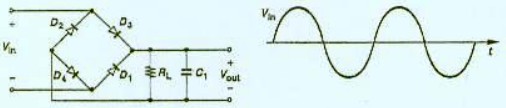

Fig.1

2. Design a self-biased common-emitter amplifier as shown in Fig.2 for voltage gain A_v = 36.5. Assume V_{CC} = 1.8 V, I_C = 2 mA, $I_S = 5 \times 10^{-16}$ A, β = 100, $V_A = \infty$. C_1 and C_2 are blocking capacitors. (a) Determine the required value of R_C and R_B. 6% (b) Calculate V_{CE}, V_{BE} and I_B. 6% (c) Plot the small signal equivalent circuit that neglects R_B . 6%　(Hint. $V_{BE} = V_T \ln(I_C / I_S)$, ln(10) = 2.303, ln(2)= 0.693 and V_T = 26 mV)　18%

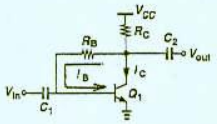

Fig.2

3. Consider the circuit as shown in Fig.3, where a source follower (M_1 and I_1) precedes a common-gate stage (M_2 and R_D). If the transconductance $g_{m1} = g_{m2}$ and λ=0 (λ is the channel-length modulation coefficient)　(a) Find the overall voltage gain. 6% (b) Determine the input and output impedance. 6% (c) Plot the small signal equivalent circuit. 6%　18%

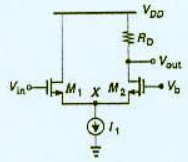

Fig.3

P149

102149

4. The CMOS operational amplifier shown in Fig. 4 has the following device geometries (in μm). (20%)

Transistor	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
W/L	20/0.5	20/0.5	5/0.5	5/0.5	40/0.5	10/0.5	40/0.5	40/0.5

Assume $I_{REF} = 100\mu A$, $V_{in} = 0.5V$, $V_{ip} = -0.5V$, $\mu_n C_{ox} = 100\mu A/V^2$, $\mu_p C_{ox} = 50\mu A/V^2$, $V_{DD} = V_{SS} = 2.5V$, $|V_A| = 10V$ for all devices. Find I_D, $|V_{OV}|$, g_m and r_o for all devices (12%). Also find the open-loop voltage gain in linear scale (8%).

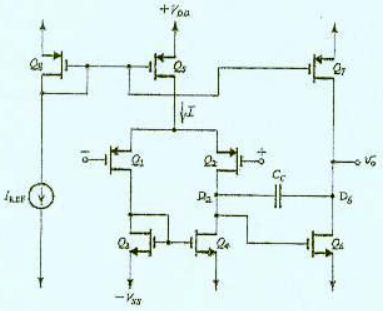

Fig. 4

5. If an amplifier has the transfer function as $T(s) = \dfrac{10s}{(1+s/10^2)(1+s/10^5)}$, please plot its magnitude Bode plot. (10%)

6. A series-shunt feedback amplifier is shown in Fig. 5. Find: (20%)
   (a) The basic amplifier gain A and the feedback factor β. (10%)
   (b) The feedback gain A_f and the voltage gain V_o/V_s. (5%)
   (c) The input resistance R_{in} and output resistance R_{out}. (5%)

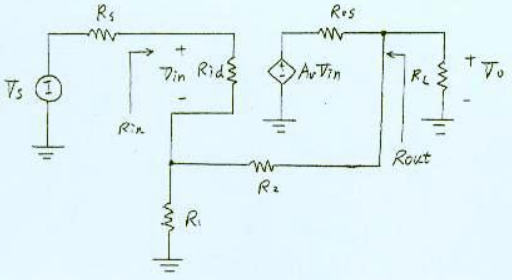

Fig. 5

P150

102150