(102)輔仁大學碩士班資格考試試題	考試日期：102 年 3 月 8 日第 3 節
	本試題共 1 頁 (本頁為第 1 頁)

科目：計算機系統　　系所組：資訊工程系

Answer all the questions clearly. Each Question is worth 10 pts for a total of 100 pts.

中英文作答均可　※注意：　試題須隨答案卷繳回。

1. **Caches and Address Translation:** Consider a 256 byte cache with 16 byte blocks, and associativity of 4 and LRU block replacement. Virtual addresses are 32 bits. The cache is physically tagged. The processor had 64KB of physical memory.
   a). What is the total number of tag bits? **(5%)**
   b). Assume each page is 64 bytes. How large would a single-level page table be given that each page requires 4 protection bits, and entries must be an integral number of bytes? **(5%)**
2. A graduate student repeatedly runs a program on an old Fu Jen Catholic University computer and records that the program took 80 seconds to execute. Of this execution time, 36% is used for memory access instructions, 44% for arithmetic instructions, and 20% for other tasks such as branch, jump and so on. Suppose, the University decides to enhance this computer, and there are two possible improvements: the first one is to make the arithmetic instructions and memory access run 4 times faster than before and the second one is to make memory access instructions run 4 times faster and other tasks to be 8 times faster. (In the second option, arithmetic instruction execution is not affected)
   a). What will the speedup be for option 1? **(4%)**
   b). What will the speedup be for option 2? **(4%)**
   c). Which option will be better? Why? **(2%)**
3. Plot the following function on a Karnaugh map. (Do not expand to minterm form before plotting.)
   F(A,B,C,D) = A′B′ + CD′ + ABC + A′B′CD′ + ABCD′
   a). Find the minimum sum of products. **(5%)**
   b). Find the minimum product of sums. **(5%)**
4. Consider executing the following code on the pipelined datapath as seen on MIPS architecture. Assume no bubble or stall while executing these instructions. (**I1 ~ I6** are instruction count)
   I1: add R1, R2, R3
   I2: add R4, R5, R6
   I3: add R7, R8, R9
   I4: add R10, R11, R12
   I5: add R13, R14, R15
   I6: lw R1, 40(R1)
   Draw the pipelined datapath.
   a). During the seventh cycle of the pipeline, which registers are being read and which register will be written? **(5%)**
   b). During seventh cycle, which instruction is executing in ALU? **(5%)**
5. Here is a series of address references given as word addresses:
   2, 3, 11, 16, 21, 13, 64, 48, 19, 11, 3, 22, 4, 27, 6, 11
   a). Assuming a direct-mapped cache with 16 one-word blocks that is initially empty, label each reference in the list as a hit or a miss and show the final contents of the cache. **(5%)**
   b). Using the series of references given above, show the hits and misses and final cache contents for a direct-mapped cache with a four-word blocks and a total size of 16 words. **(5%)**
6. What is "copy on write"? What is the main advantage of using it? **(10%)**
7. What are kernel threads? What are the advantages of using them? **(10%)**
8. Explain the idea of "paging" supported in modern operating systems. Why is it necessary? **(10%)**
9. What are "synchronous write" and "asynchronous write" in disk I/O? **(10%)**
10. What is "processor affinity"? **(10%)**

※ 注意：1.考生須在「彌封答案卷」上作答。
2.本試題紙空白部份可當稿紙使用。
3.考生於作答時可否使用計算機、法典、字典或其他資料或工具，以簡章之規定為準。