(102)輔仁大學碩士班招生考試試題	考試日期：102 年 3 月 8 日第 二 節
	本試題共 二 頁 (本頁為第 一 頁)

科目：電子學　　系所組：電機工程學系乙組

1. 選擇題 (30%)： 請標明題號，作答於彌封答案卷內。

(1) If a BJT is in active mode, which operation is true? (A)E-B junction forward, C-B junction forward. (B)E-B junction forward, C-B junction reverse. (C)E-B junction reverse, C-B junction forward. (D)E-B junction reverse, C-B junction reverse.

(2) The majority charge carriers of *p*-type and n-type silicon are (A) holes and electrons respectively. (B) electrons and holes respectively. (C) both electrons. (D) both holes.

(3) Calculate the value of g_m for a BJT biased at I_C=0.5mA. (A) 20 mA/V. (B) 10 mA/V. (C) 5 mA/V. (D) 1 mA/V.

(4) Which statement of a differential pair is true? (A) high common-mode gain. (B) high common-mode rejection ability (C) low input resistance. (D) immunize to mismatch.

(5) Which cause the gain falls off at low-frequency band of a discrete-circuit amplifier. (A) internal capacitive effects. (B) Miller's effect. (C) output loading (D) coupling and bypass capacitors.

(6) What is the feedback topology for the circuit in Fig.1? (A) Series-shunt. (B) Series-series. (C) Shunt-shunt. (D) Shunt-series.

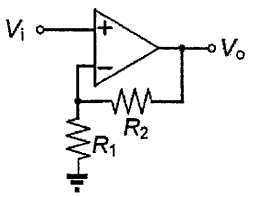

Fig. 1.

(7) For a one-pole system, the dc gain is 60dB. When apply this system as a unity gain feedback configuration, the phase margin is (A) 45°. (B) 60°. (C) 90°. (D) 180°.

(8) Which statement about a 2nd-order bandpass filter is true? (A) contains two zeros at infinite. (B) contains two zeros at origin. (C) contains one zero at origin. (D) contain one pole at origin and one zero at infinite.

(9) The condition for the feedback loop of Fig.2 to provide sinusoidal oscillations of frequency ω_0 is (A) at ω_0 the phase of the loop gain should be 180°, and the magnitude of the loop gain should be zero. (B) at ω_0 the phase of the loop gain should be zero, and the magnitude of the loop gain should be zero. (C) at ω_0 the phase of the loop gain should be 180°, and the magnitude of the loop gain should be unity. (D) at ω_0 the phase of the loop gain should be zero, and the magnitude of the loop gain should be unity.

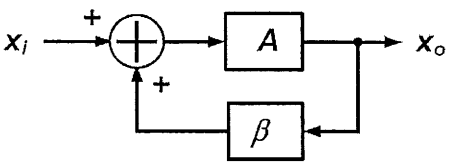

Fig. 2.

(10) If the capacitor in Fig. 3 is 1μF, and none-overlapped clock ϕ_1, ϕ_2 operate at frequency of 1kHz, the equivalent resistor between a and b is (A) 2π kΩ. (B) 1 mΩ. (C)1 kΩ. (D)1/2π mΩ

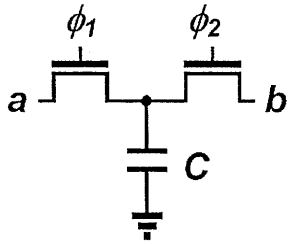

Fig. 3.

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2.本試題紙空白部份可當稿紙使用。
3.考生於作答時可否使用計算機、法典、字典或其他資料或工具，以簡章之規定為準。

2. For the circuit in Fig. 4, (15%)
   (1) derive an expression for the transfer function $V_o(s)/V_i(s)$.
   (2) design R_1, R_2, and C_2 to obtain a dc gain of 40dB, a 3-dB frequency of 1kHz, and an input resistance of 1 kΩ.
   (3) find the frequency when the magnitude of transmission becomes unity, and the phase angle at this frequency.

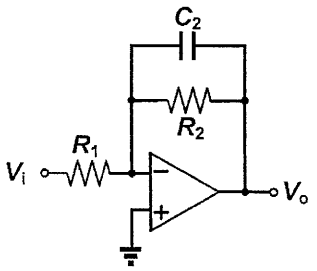

Fig. 4.

3. In Fig. 5, V_{CC}=10V, V_{BB}=3.2V, R_{BB}=10kΩ, R_C=3kΩ, and β=100, (10%)
   (1) find the dc base current, dc collector current, and dc collector voltage. (Hint: $V_{BE(on)}$≈0.7V, V_T=25mV)
   (2) determine the voltage gain v_o/v_i.

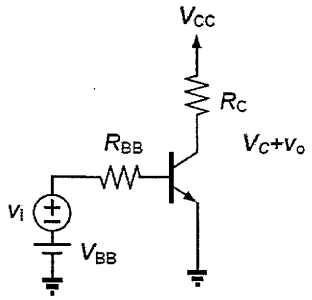

Fig. 5

4. Fig.6 shows the feedback amplifier. If the op amp has open-loop gain μ, a differential input resistance R_{id}, and an output resistance r_o. (15%)
   (1) If the loop gain is large, proof that the gain of the amplifier is $-R_F/R_S$.
   (2) Find the values of R_{in}, R_{out}, V_o/V_s for the case $\mu=10^2$ V/V, $R_{id}=\infty$, r_o=100Ω, R_F=10kΩ, and R_s=1kΩ.

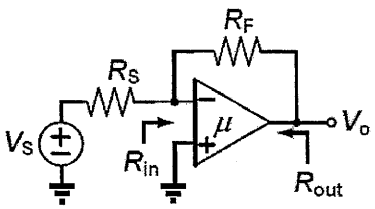

Fig. 6

5. Design the circuit in Fig.7 to realize a low-pass filter with f_0=4kHz and Q=1/$\sqrt{2}$. Use 10-kΩ resistors.(10%)

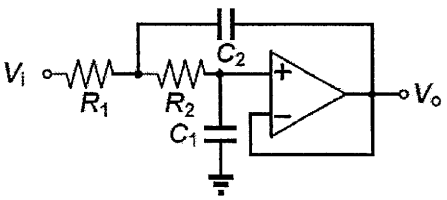

Fig. 7

6. The CMOS op amp of Fig.8 is fabricated in a process for which V'_{An}=|V'_{Ap}|=20V/μm. (20%)
   (1) Find A_v if all devices are 1μm long, V_{OV1}=0.4V, and V_{OV6}=0.5V. Also, find the op-amp output resistance obtained when the second stage is biased at 0.5mA.
   (2) If C_2=1pF, I=0.4mA, find the value of C_C that results in f_t=100MHz. What is the 3-dB frequency of the open-loop gain?

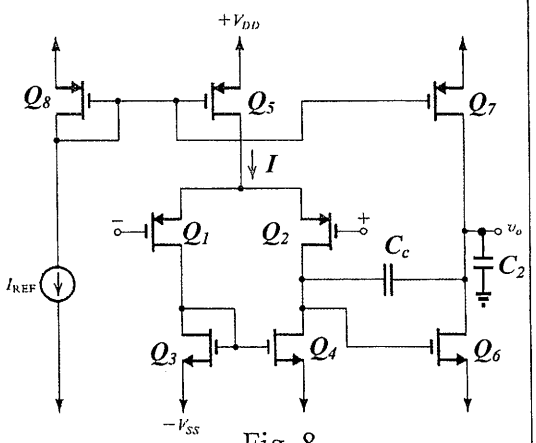

Fig. 8

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