國立高雄大學 102 學年度研究所碩士班招生考試試題

科目：計算機結構與作業系統　系所組別：資訊工程學系　是否使用計算機：否
考試時間：100 分鐘　本科原始成績：100 分

I. [20%] 單選題 (每題 2 分，共 10 題)

1. ABC Computer Company releases the ABC2 computer. It is just like ABC1 but contains an improved divider which doubles the performance of the divide instruction. If divides make up 10% of the ABC2 execution time, what is the overall speed-up with ABC2?
   (A) 1.05
   (B) 1.1
   (C) 1.5
   (D) 2
2. Given a floating point number 9.75_{ten} , what is the representation in the IEEE 754 single precision?
   (A) 0 10000010 00111000000000000000000
   (B) 0 00000011 00111000000000000000000
   (C) 0 10000010 10011100000000000000000
   (D) 0 00000011 10011100000000000000000
3. Pipelining enhances performance by
   (A) shortening instruction execution time
   (B) increasing the CPI
   (C) reordering the order of instruction execution
   (D) increasing instruction throughput
4. Which statement for cache is <u>not</u> true?
   (A) Higher associativity reduces conflict misses, but also increases hit time
   (B) Bigger caches reduce capacity misses, but potentially longer hit time
   (C) Larger blocks reduce compulsory misses, but also increase capacity misses
   (D) Multilevel caches reduce miss penalty
5. Which statement for pipelining is <u>not</u> true?
   (A) Deeper pipeline can improve instruction-level parallelism
   (B) In order to reduce branch delay, a branch target buffer caches the destination PC or destination instruction for a branch
   (C) All hazards can be resolved by stalls
   (D) Dynamic pipeline scheduling can reorder the order of instruction execution so as to avoid stall
6. What provide an interface to the services made available by an operating systems to user programs?
   (A) Interrupts (B) Traps (C) System calls (D) Application Programming Interface (API)

7. Which of the following disk head scheduling algorithms does not take into account the current position of the disk head?

   (A) SSTF (B) FCFS (C) LOOK (D) SCAN

8. Which of the following instructions should be privileged?

   (A) Clear memory

   (B) Read the clock

   (C) Issue a trap instruction

   (D) Switch from user to kernel mode

9. Which technique allows a portion of a virtual address space to be logically associated with a file?

   (A) Shared memory

   (B) Slab allocation

   (C) Copy-on-write

   (D) Memory-mapping

10. Which statement for spinlock is true?

    (A) It is never advantageous.

    (B) It will ultimately result in a context switch when a process must wait on a lock.

    (C) It is useful when locks are expected to be held for long amounts of time.

    (D) It does not require a context switch when a process must wait on a lock.

II. [20%] 填充題：填入適當的**英文**術語 (每題 2 分，共 10 題)

1. ____1____ is a small memory that is indexed by the lower portion of the address of the branch instruction and that contains one or more bits indicating whether the branch was recently taken or not.
2. ____2____ is a method of resolving a data hazard by retrieving the messing data element from internal buffers rather than waiting for it to arrive from programmer-visible registers or memory.
3. ____3____ is a cache structure in which each memory location is mapped to exactly one location in the cache.
4. ____4____ is the buffer that holds results in a dynamically scheduled processor until it is safe to store the results to memory or a register.
5. ____5____ is the time required to fetch a block into a level of the memory hierarchy from the lower level.

6. Java compiler produces an architecture-neutral code output (.class), called _____6_____, that will run on any implementation of the Java virtual machines (VM).
7. A _____7_____ is defined as an endpoint for communication for a pair of processes to communicate over a network, and is identified by an IP address concatenated with a port number.
8. _____8_____ semantics represent an important criterion for evaluating any file system that supports file sharing and specify how multiple users of a system are to access a shared file simultaneously.
9. Consider a 32-bit address for a two-level paging system with an 4 KB page size. The outer page table has 1024 entries. The number of bits required to represent the second-level page table is _____9_____.
10. Consider the following four processes, with the length of the CPU burst given in milliseconds:

Process	P1	P2	P3	P4
Arrival Time	0	2	4	6
Burst Time	8	4	3	5

The averaging waiting time of nonpreemptive shortest-job-first (SJF) scheduling is _____10_____ milliseconds more than that of shortest-remaining-time-first (SRTF) scheduling.

III. [60%] 問答題 (每題 10 分，共 6 題)

1. Explain the following terms: (a) Spatial locality (b) *n*-way set associative (c) Average memory access time (d) Data hazard
2. The five stages of MIPS pipeline are IF (instruction fetch), ID (Instruction decode and register read), EXE (Execute operation or calculate address), MEM (Access memory operand), and WB (Write result back to register). Given the following sequence of instructions:

```
lw $2, 8($0)
lw  $3, 16($0)
add $4, $2, $3
sw $4, 24($0)
```

Suppose the data hazards must be resolved by “stalling” the dependent instructions until the needed operand is written back to the register file. We assume that when the needed operand is written back to the register file, the dependent instruction can read the needed operand from the register file in the same clock cycle. How many cycles does it take for the processor to execute these four instructions? Please give a graphical representation of your solutions.

3. Assume that a two-way set-associative cache of 64K blocks, 4-word block size, and a 32-bit address. How many total bits are required for the cache?

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4. Consider protections with access control in a UNIX system.
   (a) What are the three classifications of users in connection with each file or directory?
   (b) Either a file or a directory of each classification is associated with the three bits rwx. What do the bits mean for a file and a directory individually?

5. Two pieces of codes given below will double all **4-byte** integer elements of a **256x256** matrix mB to matrix mA. How many page faults would occur for Program1 and Program2 in the following systems with LRU page replacement algorithm?

int mA[256,256], mB[256,256];
Program1():
for (j = 0; j < 256; j++)
for (i = 0; i < 256; i++)
mA[i,j] = mB[i,j]*2;
	int mA[256,256], mB[256,256];
	Program2():
	for (i = 0; i < 256; i++)
	for (j = 0; j < 256; j++)
	mA[i,j] = mB[i,j]*2;

   (a) Consider a computer system with 1-KB page size and each process is allocated with ***two*** frames specifically for the matrices.
   (b) Reconsider the above computer system with 1-KB page size, but each process is allocated with ***eight*** frames specifically for the matrices.
   (c) Consider another computer system with 4-KB page size and each process is allocated with ***two*** frames specifically for the matrices.

6. Redundant arrays of independent disks (RAIDs) are used for their higher reliability and higher data-transfer rate.
   (a) RAIDs are classified according to levels. Explain RAID level 0 and RAID level 1.
   (b) Comparing to RAIDs with arrays of hard-disk drives (HDD), is it worthy to use arrays of solid-state drives (SSD)? Why?
   (c) Reconsidering the previous question, is it worthy to use arrays of storage servers? Why?