1. (10%) Fig. P1 shows an NMOS transistor with its drain and gate terminals connected together. Find the $i-v$ relationship of the resulting two-terminal device in terms of the MOSFET parameters $k_n = k_n'(W/L)$ and V_{tn}. Neglect channel-length modulation.

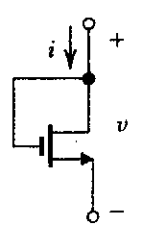

Fig. P1

2. (20%) Fig. P2 shows an ideal voltage amplifier having a gain of -100 V/V with an impedance Z connected between its output and input terminals. Find the Miller equivalent circuit when Z is (a) a 1-MΩ resistance (b) a 1-pF capacitance. In each case, use the equivalent circuit to determine V_o/V_{sig}.

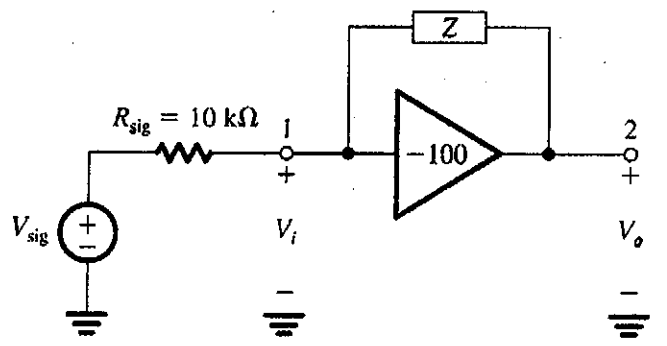

Fig. P2

3. (20%) Fig. P3 shows a positive-feedback circuit. (a) Find the loop transmission $L(s)$ and the characteristic equation. (b) Sketch a root-locus diagram for varying K, and find the value of K that makes the circuit oscillate.

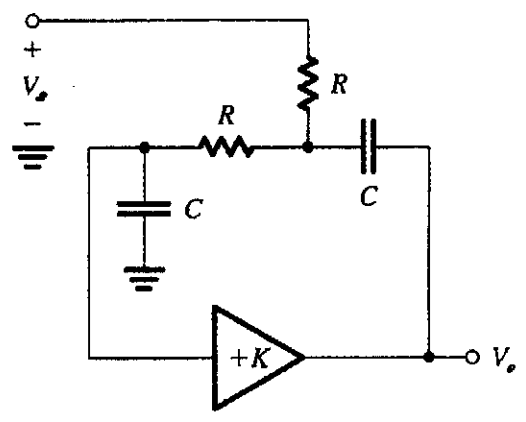

Fig. P3

4. The operational amplifier (OPA) shown in Fig. P4 is an ideal OPA, and the switches $S_{i|i=1\sim N}$ are controlled by the controlling signals $b_{i|i=1\sim N}$, respectively.
   (a) Please derive the output V_o using known parameters V_{REF}, R, and $b_{i|i=1\sim N}$. (10%)
   (b) In the case of V_{REF} = 2 V, what the minimum bit number (N) of b_i is required to generate an output (V_o) of -1.8125 V and what is the corresponding $b_{i|i=1\sim N}$. (5%)

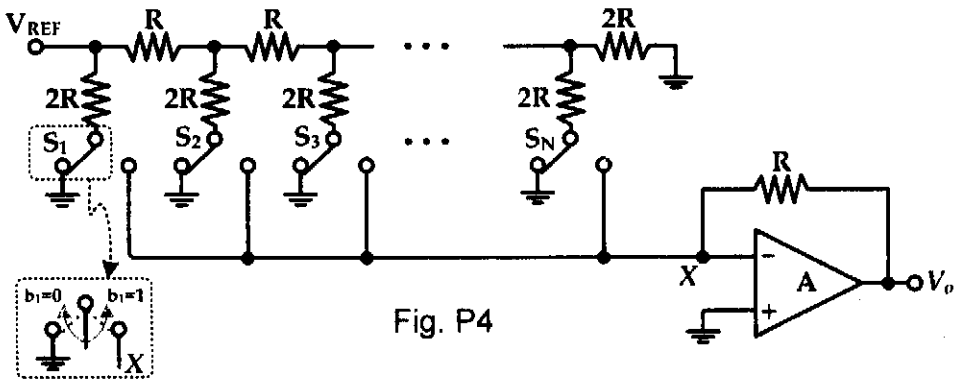

Fig. P4

5. Consider the voltage regulation circuit shown in Fig. P5 for the case of V_{in} = 10 V. Assume the diode D_1 to have a 0.7-V drop at 5 mA current while D_2 is a 6.8-V zener diode with a 6.8-V drop at 5 mA current, and an incremental resistance of 20 Ω. (Note: thermal voltage V_T = 25 mV)
   (a) Determine the line regulation ($\Delta V_O/\Delta V_{in}$). (6%)
   (b) Determine the load regulation ($\Delta V_O/\Delta I_L$). (6%)

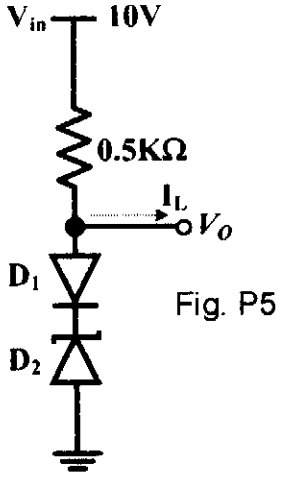

Fig. P5

6. (a) Please sketch the input/output characteristic of a logic inverter, also explain the concepts of noise margin using the input/output characteristic. (5%)
   (b) Fig. P6 shows an inverter circuit, please find the output high level (V_{OH}) and output low level (V_{OL}). Assume that PMOS transistor Q has the (W/L) ratio of 100, $\mu_p C_{OX}$ = 50 μA/V², λ_p = 0 V⁻¹, and $|V_{tp}|$ = 0.8 V. (10%)

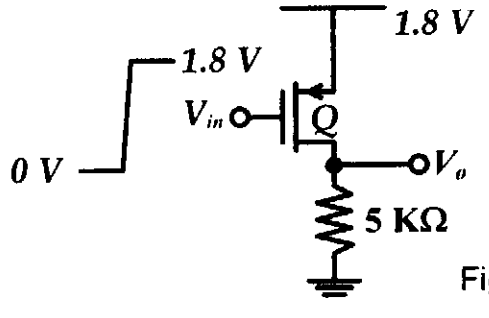

Fig. P6

7. Design a row decoder for an 8 words x 8-bit SRAM, please show the circuit in transistor level. (8%)