國立中正大學 102 學年度碩士班招生考試試題

電磁晶片組

系所別：電機工程學系-計算機工程組　　科目：電子學

晶片系統組

第 2 節

1. Figure P1 shows a differential amplifier, where the two drain resistances exhibit a mismatch ΔR_D and $R_{ss} \neq \infty$.
   (a) Please derive the common-mode rejection ratio (CMRR). (10%)
   (b) Compare to the ideal case ($\Delta R_D = 0$), explain the non-ideal effects that may happen in this circuit. (5%)

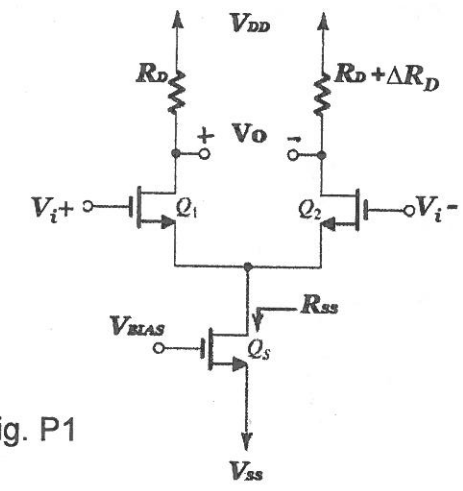

Fig. P1

2. Figure P2 shows an amplifier. The input signal v_{sig} is coupled to the gate through a very large capacitor (shown as infinite). The output voltage signal v_O that develops at the drain is coupled to a load resistance via a very large capacitor (shown as infinite).
   (a) If the transistor Q has V_t = 0.8V, and k_n = 2mA/V^2, design the bias circuits, R_1 and R_2, to establish I_D = 0.5mA. (4%)
   (b) Find g_m and r_o if V_A = 50V. (8%)
   (c) Draw a complete small-signal equivalent circuit for the amplifier, assuming all capacitors behave as short circuits at signal frequencies. (4%)
   (d) Find R_{in}, R_{out}, and v_O/v_{sig}. (9%)

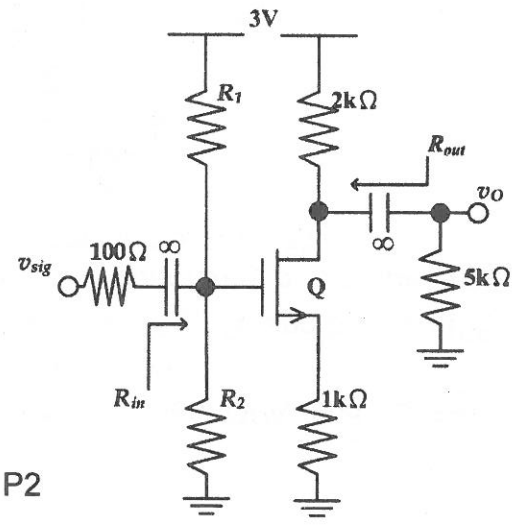

Fig. P2

3. The high-frequency response of an amplifier is characterized by two zeros at $\omega = \infty$ and two poles at ω_{p1} and ω_{p2}. For $\omega_{p2} = k^*\omega_{p1}$, find the value of k that results in the exact value of the upper 3-dB frequency, ω_H, being $0.9\omega_{p1}$.(10%)

4. The operational amplifier (OPA) shown in Fig. P4 is an ideal OPA, and the switches $S_{i|i=1\sim N}$ are controlled by the controlling signals $b_{i|i=1\sim N}$, respectively.
   (a) Please derive the output V_o using known parameters V_{REF}, R, and $b_{i|i=1\sim N}$. (10%)
   (b) In the case of V_{REF} = 2 V, what the minimum bit number (N) of b_i is required to generate an output (V_o) of -1.8125 V and what is the corresponding $b_{i|i=1\sim N}$. (5%)

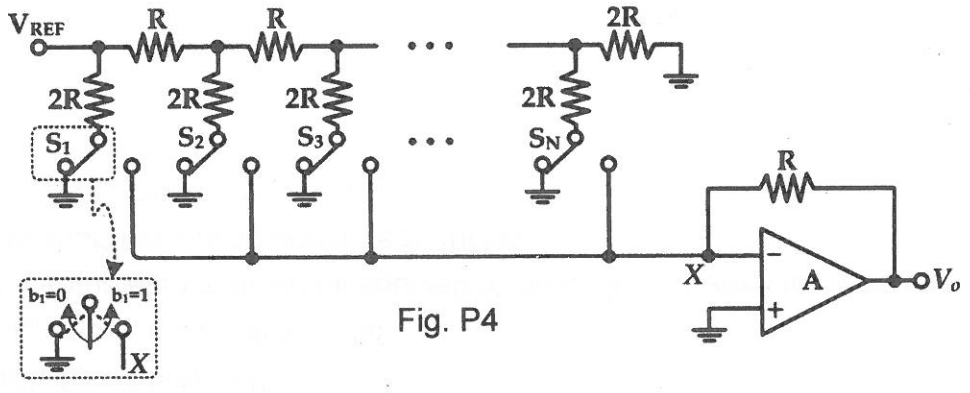

Fig. P4

5. Consider the voltage regulation circuit shown in Fig. P5 for the case of V_{in} = 10 V. Assume the diode D_1 to have a 0.7-V drop at 5 mA current while D_2 is a 6.8-V zener diode with a 6.8-V drop at 5 mA current, and an incremental resistance of 20 Ω. (Note: thermal voltage V_T = 25 mV)
   (a) Determine the line regulation ($\Delta V_O/\Delta V_{in}$). (6%)
   (b) Determine the load regulation ($\Delta V_O/\Delta I_L$). (6%)

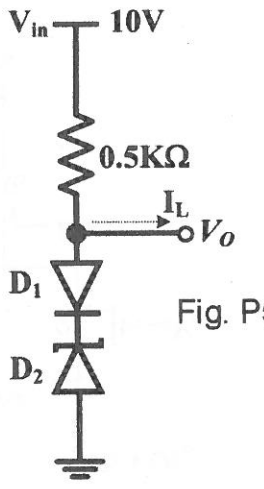

Fig. P5

6. (a) Please sketch the input/output characteristic of a logic inverter, also explain the concepts of noise margin using the input/output characteristic. (5%)
   (b) Fig. P6 shows an inverter circuit, please find the output high level (V_{OH}) and output low level (V_{OL}). Assume that PMOS transistor Q has the (W/L) ratio of 100, $\mu_p C_{OX}$ = 50 μA/V², λ_p = 0 V⁻¹, and $|V_{tp}|$ = 0.8 V. (10%)

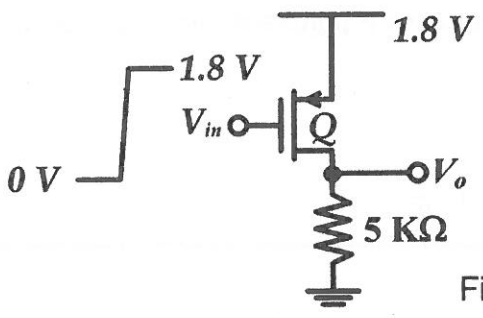

Fig. P6

7. Design a row decoder for an 8 words x 8-bit SRAM, please show the circuit in transistor level. (8%)