國立中山大學102學年度碩士暨碩士專班招生考試試題

科目名稱：電子學【光電所碩士班選考】　　題號：435004

※本科目依簡章規定「可以」使用計算機（廠牌、功能不拘）　　

(1)(20%)

(a) (5%)Please give an equation to express current flow in a semiconductor material. You should explain all the terms you give.

(b) (5%)Please write down the equation for current-voltage (I-V) relation of a pn diode and also draw a schematic of I-V relation. You should define the reversed and forward bias regimes.

(c) (10%)Please explain the basic operation principles of MOS and BJT, also write down and explain their small signal circuit models.

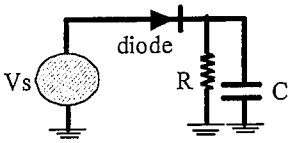

Figure 1

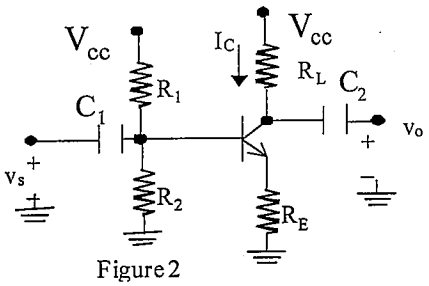

Figure 2

(2) (20%)As shown in figure 1, a diode serially connected with a resistor **R** and a capacitor **C** is served as a rectifier circuit. The voltage source **Vs** is a time-varying voltage source and the output voltage is placed across **R**.

(a) (5%)Please state the operational principle of this circuit and also plot the large signal equivalent circuit model for this circuit.

(b) (10%)If $V_s=V_o \cdot \sin(2\pi \cdot f \cdot t)$, please draw the schematic diagram of the output waveform within a period of time. V_o, f, and t are source amplitude, frequency, and time. If removing the capacitance, what is the difference in output waveform? Please explain all the plots in details.

(c) (5%)If the diode has turn-on voltage of $\mathbf{V_r}$ and series resistance of $\mathbf{R_f}$, use the large signal model to estimate the values of **R** and **C** to get output rectified DC voltage within 10% variation.

(3) (25%)In figure 2, a BJT common-emitter circuit is used for amplifier. BJT has common-base forward short-circuit gain $\alpha_F=0.98$. R_1, R_2, R_L, and R_E are 100, 10, 2, and 1KΩ respectively. $V_{CC}=12V$.

(a) (10%)Determine the operation point of BJT (i.e. I_C and V_{CE}) if ideal BJT is used. And also find the AC gain.

(b) (5%)The linearity of amplifier is quite important to amplifier operation. If the BJT is not ideal, what are the major factors leading to the nonlinearity as large input signal is coupled?

(c) (5%)What are the purposes of C_1 and C_2 in the circuit?

(d) (5%)Draw the equivalent circuit model of circuit at low-frequency and high-frequency regimes.

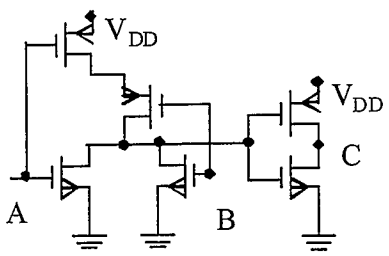

Figure 3

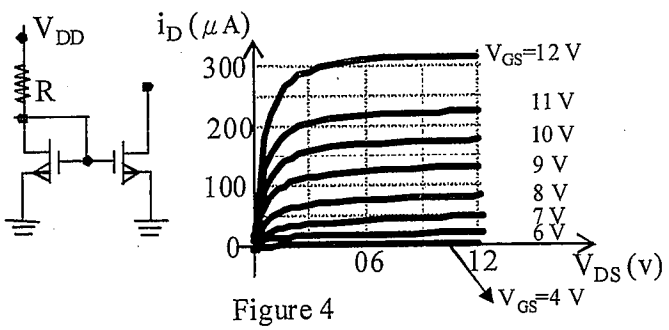

Figure 4

國立中山大學102學年度碩士暨碩士專班招生考試試題

科目名稱：電子學【光電所碩士班選考】　　題號：435004

※本科目依簡章規定「可以」使用計算機（廠牌、功能不拘）　　

(4) (15%)

(a) (5%)Please draw the cross section of CMOS circuit in IC fabrication.

(b) (10%)Figure 3 plots a CMOS logic circuit with two inputs ports, **A** and **B**, and one output port, **C**. What is the logical function of this circuit? Please verify it by truth table.

(5)(20%)As shown in figure 4, a current mirror is formed by two identical MOS transistors, where the drain current with drain-source voltage (i_D-V_{DS}) at different V_{GS} levels is also shown in figure. **R**=40kΩ and $\mathbf{V_{DD}}$=12V.

(a)(5%) Please explain how the current mirror functions.

(b)(10%) Use i_D-V_{DS} relation to find the i_D of the output transistor. Give all the details in your calculation.

(c)(5%) If the mirrored current should be scaled up to a ratio of **r** (right i_D transistor / left i_D transistor = **r**), how to scale up the geometrical structure of such two MOS transistors? Explain that.