國立中山大學102學年度碩士暨碩士專班招生考試試題

科目名稱：計算機結構【電機系碩士班丙組、己組】　　題號：431009

※本科目依簡章規定「可以」使用計算機（廠牌、功能不拘）　　

[Problem 1] Terminology Explanation (20%)
(a) Superscalar Processor (b) Pipeline Processing (c) Real Time Processing
(d) Delayed branch (e) Multi-core Processor

[Problem 2] (a) Describe the floating-point addition algorithm and hardware for IEEE 754 standard.(10%) (b)Design the adder architecture for adding two IEEE 754 floating-point numbers with the normalization form result. (10%)

[Problem 3] A set associative cache has a block size of four 32-bit words and a set size of 4. The cache can accommodate a total of 64K words. The main memory size that is cacheable is 256M * 32 bits. Design the cache structure and show how the processor' s addresses are interpreted. (20%)

[Problem 4] Briefly describe what three techniques are possible for I/O operations. (10%)

[Problem 5] (a)Given the instruction architecture as follows. (20%)

Name	Format	Example						Comments
add	R	0	18	19	17	0	32	add $s1, $s2, $s3
sub	R	0	18	19	17	0	32	sub $s1, $s2, $s3
lw	I	35	18	17	100			lw $s1, 100($s2)
sw	I	43	18	17	100			sw $s1, 100($s2)
beq	I	4	17	18	25			beq $s1, $s2, 100
bne	I	5	17	18	25			bne $s1, $s2, 100
slt	R	0	18	19	17	0	42	slt $s1, $s2, $s3
j	J	2	2500					j 1000(see section 3.8)
jr	R	0	31	0	0	0	8	jr $ra
jal	J	3	2500					jal 1000(see section 3.8)
Field size		6 bits	5 bits	5 bits	5 bits	5 bits	6 bits	All MIPS instructions 32 bits
R-format	R	op	rs	rt	rd	shamt	funct	Arithmetic instructions format
I-format	I	op	rs	rt	address			Transfer, branch format
Addi	**I**	**8**	**rs**	**rt**	**imm16**			**addi $s1, $s2, imm16**

Transfer the C program block as follows to the machine code as you can.

```
for(i=0; i<10; i++)
  A[i]= A[i]+k;
```

(Assume: Start address of 32-bit integer array *A*--> 0x1000,
Start address of 32-bit integer variable *k* --> 0x1100 and
Start address of 32-bit integer variable *i* --> 0x1104)

(b) Suppose we have made the following measurements of average CPI for instructions:

Instruction	Average CPI
Arithmetic	1.0 clock cycles
Data transfer	1.4 clock cycles
Conditional branch	1.7 clock cycles
Jump	1.2 clock cycles

Compute the effective CPI for the machine code at(a) . (10%)