※ 考生請注意：本試題可使用計算機

1. Consider the circuit shown in Figure 1 with parameters of $R_s$=10 kΩ, $R_i$=10 kΩ, $C_i$=10 pF, $R_1$=10 kΩ, $R_2$=20 kΩ, $C_1$=100 nF and $G_m$=100 mA/V.
   (a) Find $T_i(s) = V_i(s)/V_s(s)$ in the standard form of two polynomial expressions and the corresponding 3dB frequency. (6%)
   (b) Find $T(s) = V_o(s)/V_s(s)$ in the standard form of two polynomial expressions and the gain-bandwidth product. (10%)

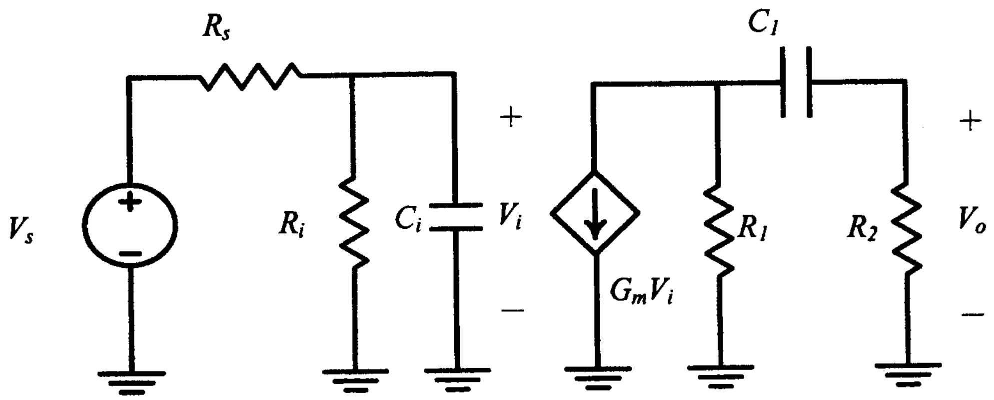


Figure 1

2. Consider the circuit shown in Figure 2 with parameters of $V_{DD}$=5 V, $\mu_n C_{ox}$= 40 $\mu$A/V$^2$, and $\mu_p C_{ox}$=20 $\mu$A/V$^2$, $|V_{tn0}|=|V_{tp0}|$=1V, $\gamma$=0.5V$^{1/2}$, $2\Phi_f$=0.6V, $(W/L)_{Q1}$=2 $\mu$m/1 $\mu$m, $(W/L)_{Qp}$=2 × $(W/L)_{Qn}$ =5 $\mu$m/1 $\mu$m, C = 10fF.
   (a) Determine threshold voltage of $Q_1$ after $v_I=V_{DD}$, $v_C=V_{DD}$ and $v_x$ is stable. (4%)
   (b) Find noise margin $V_{OH}$ of $Q_1$ when $v_I=V_{DD}$ and $v_C=V_{DD}$. (4%)
   (c) Determine the static current of the inverter, its power consumption and $v_O$ when $v_I=V_{DD}$ and $v_C=V_{DD}$. (10%)

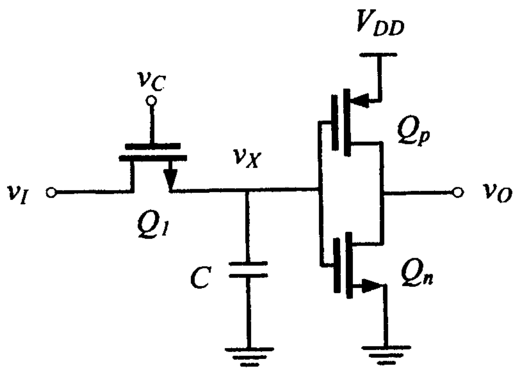


Figure 2

(背面仍有題目,請繼續作答)

※ 考生請注意：本試題可使用計算機

3. It is required to design the circuit of Figure 3 to provide a constant current $I_O$=10μA.
   (a) Determine the values of the required resistors $R_2$ and $R_3$, assuming that $I_{REF}$=100μA, $v_{BE}$=0.7V at a 1-mA current, and β to be high. (6%)
   (b) If β = 200 and $V_A$=100V, find the value of the output resistance, and find the change in output current corresponding to a 5-V change in output voltage. (6%)

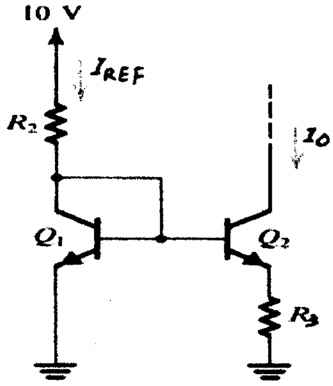


Figure 3

4. It is required to design the circuit of Figure 4 to provide a bias current $I_B$=225μA with $Q_8$ and $Q_9$ as matched devices having W/L = 60/0.5. Transistors $Q_{10}$, $Q_{11}$, and $Q_{13}$ are to be identical, with the same $g_m$ as $Q_8$ and $Q_9$. Transistor $Q_{12}$ is to be four times as wide as $Q_{13}$. Let $\mu_nC_{ox} = 3\mu_pC_{ox}$ = 180 μA/V$^2$ and $V_{DD}$=$V_{SS}$= 1.5V.
   (a) Find the required value of $R_B$ and the voltage drop across $R_B$. (4%)
   (b) Specify the W/L ratios of $Q_{10}$, $Q_{11}$, $Q_{12}$, and $Q_{13}$. (3%)
   (c) Give the expected dc voltages at the gates of $Q_{12}$, $Q_{10}$, and $Q_8$. (6%)

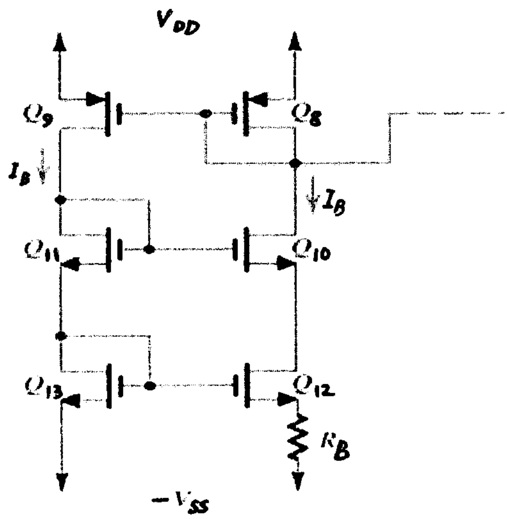


Figure 4

※ 考生請注意：本試題可使用計算機

5. Consider a feedback amplifier for which the open-loop gain A(s) is given by

$$A(s) = \frac{1000}{(1+s/10^4)(1+s/10^5)^2}$$

If the feedback factor β is independent of frequency, find the frequency at which the phase shift is 180°, and find the critical value of β at which oscillation will occur. (8%)

6. An amplifier has a dc gain of $10^5$ and poles at $5 \times 10^5$ Hz, $10^7$ Hz, and $5 \times 10^8$ Hz. To stabilize the amplifier with unity feedback ($\beta = 1$), move the first pole by introducing a compensation capacitor. Assume the second pole remains. Calculate the frequency of the first new pole to achieve a phase margin of $45^{\circ}$. (5%)

7. A prototype active filter with admittances $Y_1$ through $Y_4$ is shown in Figure 7a. Assume the Opamp is ideal. The transfer function of this filter is as follows

$$\frac{v_o(s)}{v_i(s)} = \frac{Y_1 Y_2}{Y_1 Y_2 + Y_4(Y_1 + Y_2 + Y_3)}$$

A designed filter is the cascade of the prototype circuits shown in Figure 7b, where R = 10 kΩ, C = 0.01 μF, $C_1 = 1.082C$, $C_2 = 0.9241C$, $C_3 = 2.613C$, $C_4 = 0.3825C$

(a) Calculate the zeros and poles of the transfer function for this designed filter. (8%)

(b) What is the type of this filter (lowpass, highpass, bandpass, bandreject, or ….)? Explain why? (5%)

(背面仍有題目,請繼續作答)

※ 考生請注意：本試題可使用計算機

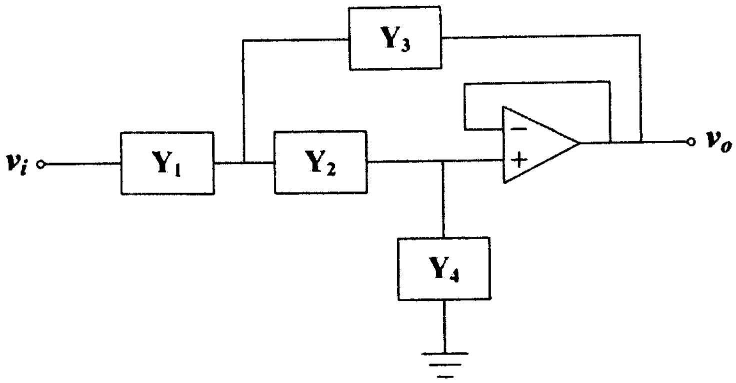


Figure 7a

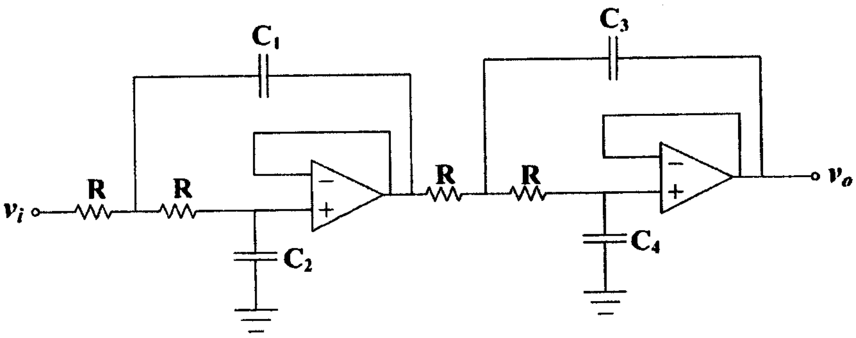


Figure 7b

8. A phase-shift oscillator is shown in Figure 8, where R = 10 kΩ, C = 10 nF
   (a) Find the loop gain by breaking the circuit at node X. (10%)
   (b) Calculate the oscillation frequency $f_o$, and the minimum required value of $R_f$ for oscillation to start in this circuit. (5%)

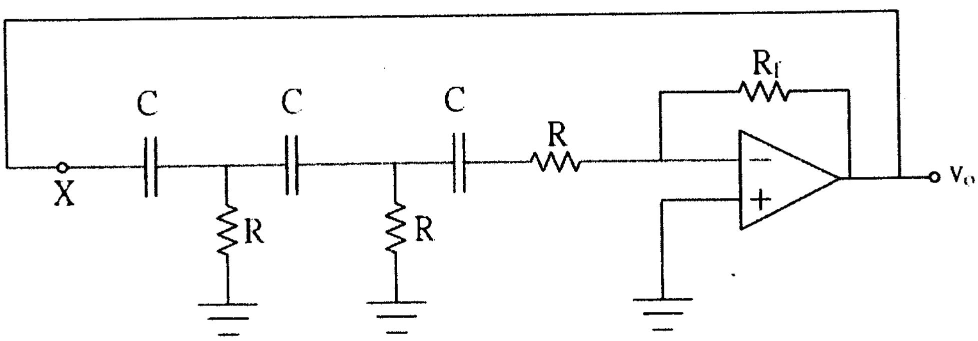


Figure 8