※ 考生請注意：本試題不可使用計算機

1. Figure 1 shows the control of the multicycle MIPS precessor. There are a number of typos in the plot. Identify and correct the typos. (20%)

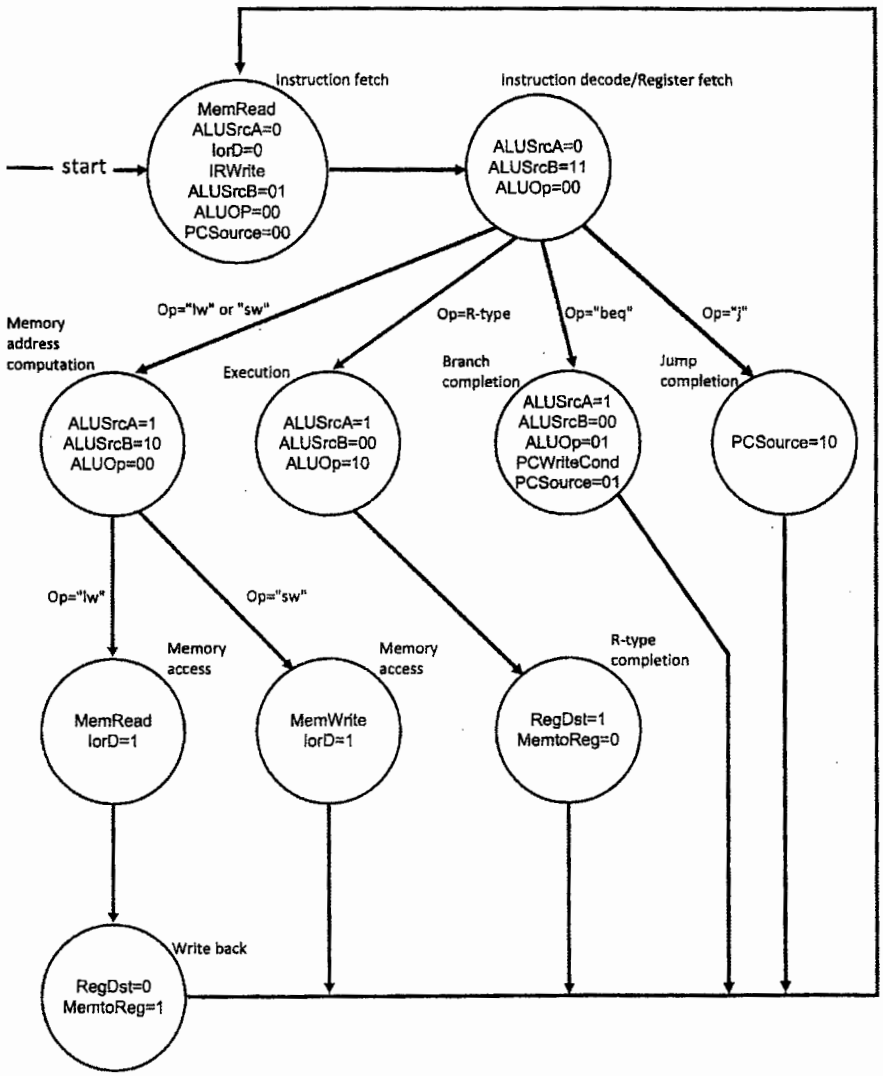

Figure 1: The control of the multicycle processor

(背面仍有題目,請繼續作答)

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2. Let the value of the program counter (i.e.,PC) be **0XCF02DA00**. What is the target address of the instruction, **j 0X20**? (20%)

3. Translate the **beq** instruction shown in the following codes into a 32-bit binary instruction, provided that the opcode of **beq** is **0X04**. (10%)

```
Loop:  add  $8,$9,$10
       add  $8,$9,$10
       add  $8,$9,$10
       add  $8,$9,$10
       add  $8,$9,$10
       add  $8,$9,$10
       add  $8,$9,$10
       beq  $0,$9,Loop
End:   add  $9,$0,$9
```

4. Consider the assembly codes as follows. Assume that the starting address of the first instruction is 10000 in the decimal notation. Translate the first instruction into corresponding machine codes, given that the opcode of **beq** is 000100 in binary notation. (10%)

```
Loop:  beq  $9,$0,End
       add  $8,$8,$10
       addi $9,$9,$-1
       j    Loop
End:
```

5. Assume that the opcodes of the **add**, **addi**, and **lw** instructions are respectively 000000, 001000 and 100011 in the binary notation. Translate the following MIPS machine codes into corresponding assembly codes. (30%)

   (a) 00000001001010100100000000100000

   (b) 00100010110101011111111111001110

   (c) 10001101001010000000010010110000

6. In a memory system, there is one TLB, one physically addressed cache, and one physical main memory. Assuming all memory addresses are translated to physical addresses before the cache is accessed. Which of the following events are **impossible** in memory system? (10%)

	Cache	TLB	Page Table
(a)	Hit	Miss	Miss
(b)	Miss	Hit	Hit
(c)	Miss	Miss	Hit
(d)	Miss	Hit	Miss