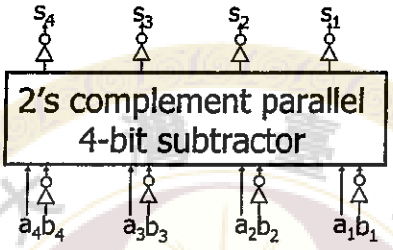
國立臺灣大學 102 學年度碩士班招生考試試題

Please provide a full and clear explanation for EVERY question; otherwise, NO point is given.

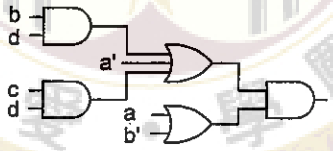
1. (10%) It is possible to find an input assignment such that the following Boolean function holds true. True or False? Please explain.
   $(A+B'+D)(E+F')(A'+B+C)(A+B+C'+E'+F)(D+E'+F')(B+C'+D'+F)=1$
2. (10%) Suppose that we have a parallel 4-bit subtractor circuit that performs subtraction of two signed 4-bit numbers in 2's complement. The following circuit computes A+B in 2's complement. True or False? Please explain. Suppose a_4 and b_4 are the most significant bits.



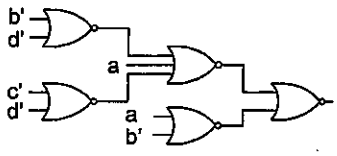
$A=a_4a_3a_2a_1$
$B=b_4b_3b_2b_1$

Fig. 1

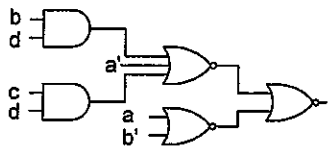
3. (10%) Define X⊗Y = XY+Y' , then G= (X⊗Y)' + (W' ⊗Z) + (XW) ⊗Y = XY, True or False? Note that the priority of ⊗ is the same as AND.
4. (10%) The ⊗ logic operation defined in problem 3 is functionally complete. True or false?
5. (10%) Use Boolean algebra to find the minimum product-of-sum expression.
   $(W+Y'+V+K)(W+Y+U+K)(W'+X+K)(W+X+Y'+Z'+K)(X+Y'+V+K)(W+Y'+V'+K)$
6. (10%) Let $H(a,b,c,d) = \Pi$ M (1, 2, 5, 7, 8, 10, 11, 13, 14, 15). Suppose that a is the most significant bit. That means, $abcd$ = 1000 corresponds to minterm m_8. Show the Shannon expansion of H with respect to d. Show your answer in minterm expansion.
7. (10%) For the following target circuit,



which of the four circuits (1~4) are equivalent to the target circuit?



(1)



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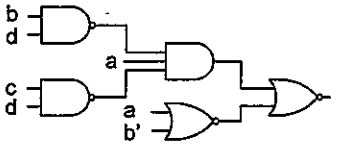

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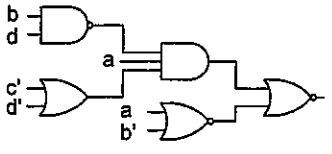

(4)

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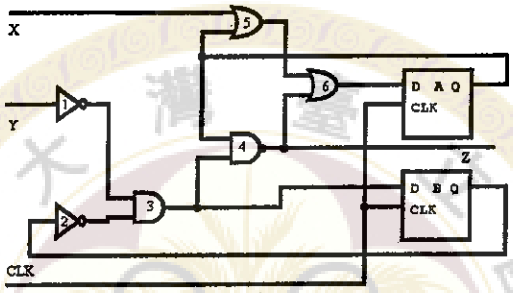
8. (10%) The following sequential circuit has two inputs (X, Y) and two D flip-flops (A, B) and one output (Z).
   a) Please fill in the state table of this circuit. Use S0, S1, S2 and S3 in the next state. (5 %)
   b) Suppose the initial state is S0. Find a shortest input sequence of XY to bring the circuit to state S2. If this is impossible, please explain. (5%)

Present state	Next state	Present output Z
S0 (AB=00)	(please use S0 S1, S2 S3 to fill in)	
S1 (AB=01)		
S2 (AB=10)		
S3 (AB=11)		



9. (10%) Use three flip-flops (*A, B, C*) and PLA to design a counter. The outputs of three flip-flops generate this sequence: Q_A, Q_B, Q_C =000, 101, 100, 110, 011, 000, … Suppose we use T flip-flop for Q_A, SR flip-flop for Q_B, and JK flip-flop for Q_C. Simplify every input equation to minimum SOP and answer the following question.
   a) Please fill in the Programmable Logic Array (PLA) Table to implement the function. (5%)

Q_A	Q_B	Q_C	T_A	S_B	R_B	J_C	K_C
…	(add	more	rows	if	needed	)	

   b) If the initial state of this counter is 111, what would happen to the next state? (5%)

10. (10%) Please deign a sequential circuit which has two one-bit inputs (X, Y) and a one-bit output (Z). Inputs X and Y represent two positive binary numbers. The least significant bit is applied in the first cycle, and the most significant bit is applied in the third cycle. (That means, '100' represents number 1, while '001' represents number 4.) Output *Z* becomes one in the third cycle if and only if $X=Y+3$; otherwise, $Z=0$. For example:

X	001	010	011	111	…
Y	100	111	110	001	…
Z	001	000	001	001	…

   a) Draw the Mealy state graph of this circuit. Please reduce to minimum state. (5%)
   b) Please fill in the following table. (5%)

State	Meaning
S0	Initial state
S1	First bit applied, X≠Y+3
S2	Second bit applied, X≠Y+3
S3	First bit applied, X=0, X=Y+3 is possible
S4	First bit applied, X=1, X=Y+3 is possible
S5	Second bit applied, _____ (please fill)
S6	Second bit applied, _____ (please fill)
…	(add more states if needed)

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