※ 注意：請於試卷內之「非選擇題作答區」標明題號依序作答。

Multiple choices questions: (total 35%)

1. (5%) Because metal-oxide-semiconductor field effect transistor (MOSFET) has been widely used in most circuit design, it is important to grab a rough idea about different kinds of single stage amplifier topography. Which of the following are truths:
   (a) The common-drain amplifier is usually the basic infrastructure for a buffer amplifier,
   (b) The common-gate amplifier has limited applications because of its low input resistance and bad high-frequence response,
   (c) The common-source amplifier with a source resistance has better frequency response in a trade-off reducing gain,
   (d) Ideally, a common-drain amplifier has the best input resistance and output resistance for voltage amplification,
   (e) To achieve a better frequency performance and moderate voltage amplification, a common-source with a source resistance topography can be used.

2. (5%) Both bipolar junction transistor (BJT) and MOSFET are typically used in various integrated circuit design. As a consequence, picking up a right type of transistor is essential. Please identify which of the following statement are truths:
   (a) The early effect of a BJT is because of the channel length modulation effect,
   (b) One of the circuit design parameter for MOSFET is W/L ratio, similarly, the circuit design parameter for BJT is the junction area of collecter-base junction,
   (c) To have a relatively thermal-stable circuit, in general, using MOSFET is better than using BJT,
   (d) The major carrier transportation mechanism in BJT is diffusion,
   (e) To have a better frequency response in the same circuit design, BJT is preferred because of less miller effect compared with MOSFET

3. (5%) A differential pair is a commonly used amplifier configuration. Following are some statements related to a differential pair circuit. Please name the correct ones.
   (a) To extend the linear range of MOSFET differential pair operation under the same bias current, we can increase to a larger V_{OV} at the expense of reducing the gain,
   (b) To increase the gain, we can increase the bias current. However, this will cause the problems of power consumption and bandwidth,
   (c) To increse the common-mode rejection ratio (CMRR), a good bias current source to have high output resistance is necessary,
   (d) Because of the existance base current, the input bias current of BJT differential pair is worse than that of MOS differential pair.
   (e) With active load, we can increase the voltage gain by sacrificing CMRR.

4. (4%) Which of the following is not true:
   (a) a Group III element introduces holes and creates P-type silicon,
   (b) E_g (band gap) can be determined from the minimum energy of photons that (are absorbed by the semiconductor,
   (c) Fermi function is the probability of an energy state being occupied by an electron,

見背面

(d) None of above

5. (4%) Which of the following is not true:
(a) 1eV equals to 1.6e-19 joules; (b) 1 KT equals to 0.0259eV at 300 K; (c) the band gap energy of SiO2 is 8 eV; (d) the density of states effective masses of Si is smaller than Ge at 300 K

6. (4%) In a simple cubic lattice with lattics constant a, the density of atoms (number per unit area) whose centers lie on a (100) surface is: (a) 1/a; (b) $1/a^2$; (c) $4/a^2$; (d) a^2

7. (4%) A silicon sample is doped with 10^{16} donors and 5 X 10^{15} acceptors per cm^3. At room temperature, the hole density is: (a) $5x10^3/cm^3$; (b) $1x10^4/cm^3$; (c) $2x10^4/cm^3$; (d) $5x10^{15}/cm^3$; (e) $1x10^{16}/cm^3$; (f) $2x10^{16}/cm^3$

8. (4%) A p-type silicon sample is uniformly doped with $N_A=10^{15}/cm^3$ and uniformly illuminated such that $\Delta n=\Delta p= 10^{14}/cm^3$. Calculate the resistivityt of the illuminated sample. Assume μ_n=1350 cm^2/V-sec and μ_p=460 cm^2/V-sec. (a) 9.75 ohm-cm; (b) 10.5 ohm-cm; (c) 13.6 ohm-cm; (d) 46.3 ohm-cm

Short answers and calculations:

1. Analyze the following OP amp circuit (Fig. 1) comprising of a signal source, a load, and one stage of amplification with R_s= 2.2 kΩ, R_1= 1 kΩ, R_F= 8.7 kΩ, R_L= 20 Ω. OP Amp specification: r_i= 2 MΩ (input resistance), r_o= 25 Ω (output resistance), μ= 200,000 kΩ (open loop voltage gain).
(i) What is the equivalent circuit model of the ideal and noideal op amp? (5%)
(ii) Derive an expression and value of the input resistance v_i/i_i of the circuits, assuming the op amp is not ideal. (10%)
(iii) Determin the value of the input resistance assuming the op amp is ideal. (5%)

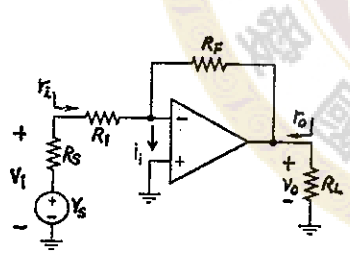

Figure 1.

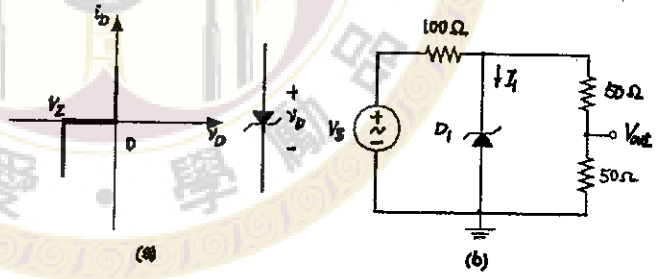

Figure 2.

2. A Zener diode ideal i-v curve is shown in Fig. 2. (a). Given a Zener voltage V_z=7.7V, find the output vltage V_{out} for the circuit of (b) when Vs is (i) 12V; (ii) 20V (10%)

3. For the amplifier circuit shown in Figure 3, the NMOS transistor has the following parameters: W/L = 0.9μm/0.18μm, μ_nC_{ox} = 1600 $\mu A/V^2$, threshold voltage V_{TN} = 0.5 V, and V_A = 10 V. Both capacitors are coupling capacitors.
(i) Calculate the DC operation point of the amplifier (find V_G, V_D, and I_D). (6%)
(ii) Find the amplifier gain (V_{out}/V_{in}). (6%)
(iii) If the resistor R_G is changed to 10 kΩ, how does this affect the DC operating point? What is the amplifier gain (V_{out}/V_{in}) now? (8%)

接次頁

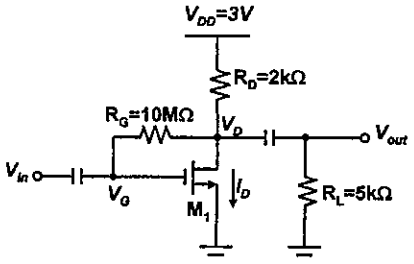

Figure 3.

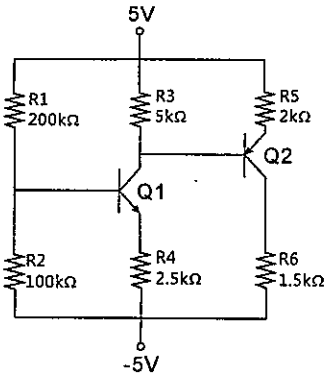

Figure 4.

4. (15%) Consider a multistage BJT circuit shown as Fig. 4. Please calculate the dc voltages at each node and the dc currents through the elements. In addition, please also calculate the open-circuit voltage gain of this circuit.

試題隨卷繳回