※ 考生請注意：本試題可使用計算機，並限「考選部核定之國家考試電子計算器」機型

1. Determine true or false for statements related to devices BJT and MOSFET. If false, please briefly explain to get full credits. (12%)
   (1) BJT and MOSFET are both three-terminal devices.
   (2) The emitter current of BJT is solely controlled by the BASE terminal while the drain-to-source current of MOSFET is only controlled by the GATE terminal.
   (3) The current of BJT and MOSFET in active mode/saturation region are both driven by majority carriers in the respective device.
   (4) Generally speaking, the current driving strength of BJT device is stronger than that of MOSFET with the same device dimension.
   (5) There are parasitic diodes in both BJT and MOSFET devices.
   (6) Einstein relationship can be applied to both BJT and MOSFET devices.

2. A particular MOS inverter has the following transfer characteristic curve as shown in Fig. 1 , where *Vo* is the output voltage and *Vi* is the input voltage. What are the values for V_{OH}, V_{OL}, V_{IH}, V_{IL}, NM_H and NM_L that are used to define noise margin? (8%)

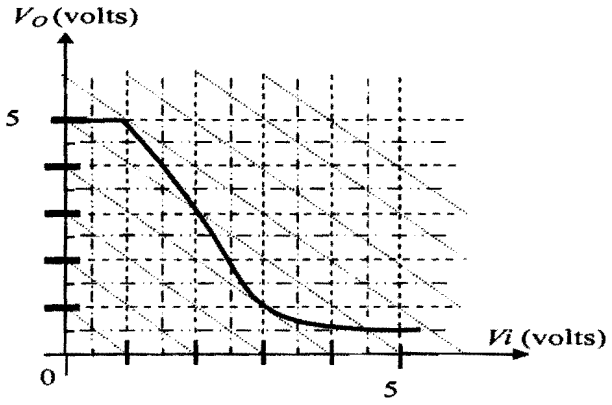

Fig. 1

3. For the MOSFET circuit shown in the Fig. 2, determine the specified output voltage under difference cases. Consider the long-channel process technology for which $|V_{tn}| = |V_{tp}| = 1$ V, $t_{ox} = 8$ nm, $\mu_n = 450 cm^2/V \cdot s$, $\mu_p = 150 cm^2/V \cdot s$, $\varepsilon_{ox} = 4.0 \times 10^{-11}$ F/m, $(W/L)_1 = 4\mu m/0.8\mu m$, $V_{DD} = 5$V. The subscript 1 & 2 stand for parameters related transistor Q1 & Q2, respectively. Channel-length modulation effect can be ignored here. (13%)
   (a) What are the values of k'_n and k'_p including their unit?
   (b) Assume $k'_p(W/L)_2 = k'_n(W/L)_1$, find v_O when $v_I = 0$V and $v_I = 5$V, respectively.
   (c) Assume $k'_p(W/L)_2 = 0.01k'_n(W/L)_1$, find v_O when $v_I = 2.5$V.

(背面仍有題目,請繼續作答)

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4. For the circuit shown in Fig. 3, the relative transistors areas are $A_{Q1}=A_{Q2}=A_{Q3}=A_{Q4}=A_{Q6}=1$. Assume that $v_{BE}\cong 0.7V$ and β is very large for all transistors. Please find the value of resistors (R_1, R_2 and R_3) and A_{Q5} to achieve $I_2=1mA$, $I_3=50\mu A$, $I_5=3mA$, and $I_6=100\mu A$. (12%)

5. An active-loaded MOS differential amplifier is shown in Fig. 4. The NMOS transistor parameters are $V_t=+2V$, V_A(channel length modulation voltage)=-40V, and $V_{GS}=+4V$ at $I_D=1mA$; The PMOS transistor parameters are $V_t=-3V$, $V_A=+40V$, and $V_{GS}=-6V$ at $I_D=1mA$. Please calculate G_m, R_o(output resistance), A_d (differential gain), and A_c (common-mode gain) (12%).

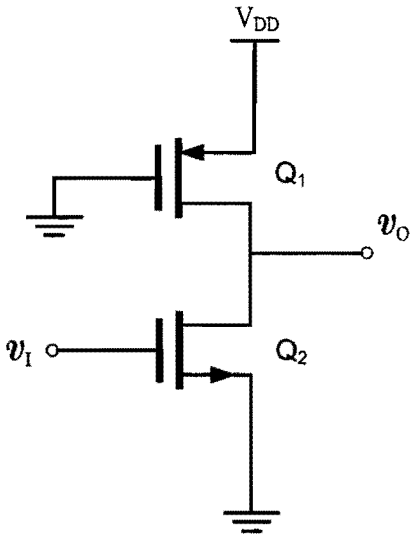

Fig. 2

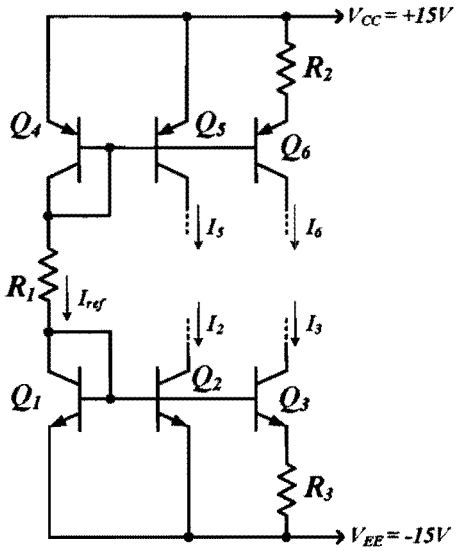

Fig. 3

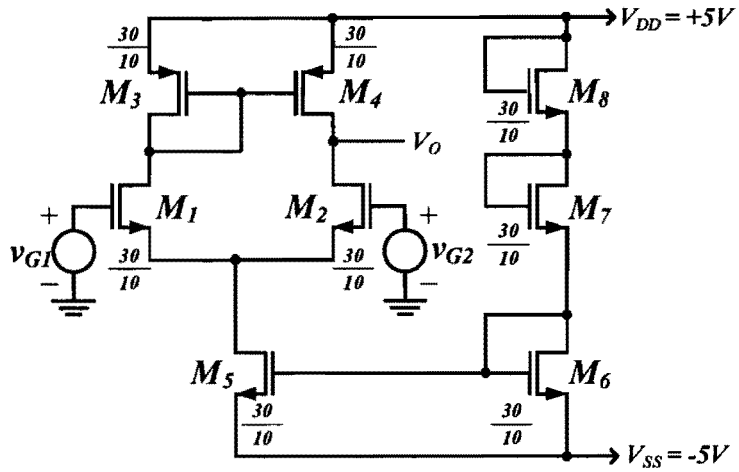

Fig. 4

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6. A single-pole op amp has a dc gain of 100 dB and a unity-gain frequency of 10 MHz.
   (a) What is the upper-cutoff frequency of the op amp itself? (3%)
   (b) If the op amp is used to build a noninverting amplifier with a closed-loop gain of 60 dB, what is the bandwidth of the feedback amplifier? (3%)
   (c) Write an expression for the transfer function of the noninverting amplifier. (3%)
7. A two-stage CMOS Opamp circuit is shown in Fig. 5, ± 1.65 V power supplies are used and all transistors except for Q_6 and Q_7 are operated with overdrive voltages of 0.2 V magnitude; Q_6 and Q_7, use overdrive voltages of 0.5 V magnitude. The fabrication process provides $V_{tn} = |V_{tp}| = 0.5$ V. If the first-stage bias current I = 200 μA, C = 1.6 pF.
   (a) Find the input common-mode range and the range allowed for V_o. (6%)
   (b) Draw the simplified circuit model for the slewing process. (5%)
   (c) Calculate the slew rate of this Opamp. (5%)
8. Consider a circuit as shown in Fig. 6 assuming the Opamp to be ideal. Let C_1 = 0.001 μF, C_2 = 0.0047 μF, R_1 = 10 kΩ, R_2 = 20 kΩ.
   (a) Derive the transfer function V_o/V_i. (9%)
   (b) Plot the frequency response of the transfer function and explain the function of this circuit. (9%)

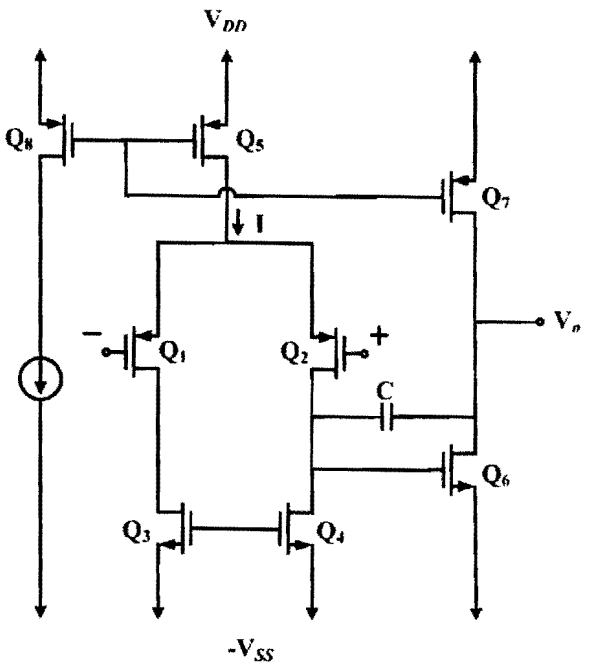

Fig.5

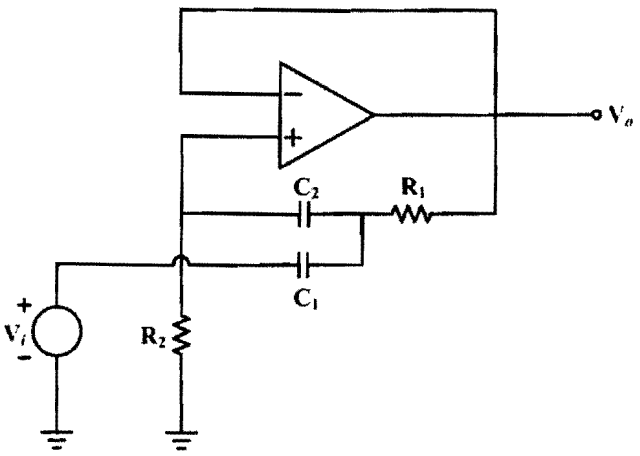

Fig.6