國立中山大學113學年度
碩士班暨碩士在職專班招生考試試題

科目名稱：計算機結構【電機系碩士班己組】

—作答注意事項—

考試時間：100分鐘

- **考試開始鈴響前不得翻閱試題，並不得書寫、劃記、作答。**請先檢查答案卷（卡）之應考證號碼、桌角號碼、應試科目是否正確，如有不同立即請監試人員處理。
- **答案卷限用藍、黑色筆(含鉛筆)書寫、繪圖或標示**，可攜帶橡皮擦、無色透明無文字墊板、尺規、修正液（帶）、手錶(未附計算器者)。每人每節限使用一份答案卷，請衡酌作答。
- 答案卡請以2B鉛筆劃記，不可使用修正液（帶）塗改，未使用2B鉛筆、劃記太輕或污損致光學閱讀機無法辨識答案者，後果由考生自負。
- 答案卷（卡）應保持清潔完整，不得折疊、破壞或塗改應考證號碼及條碼，亦不得書寫考生姓名、應考證號碼或與答案無關之任何文字或符號。
- 可否使用計算機請依試題資訊內標註為準，如「可以」使用，廠牌、功能不拘，唯不得攜帶書籍、紙張（應考證不得做計算紙書寫）、具有通訊、記憶、傳輸或收發等功能之相關電子產品或其他有礙試場安寧、考試公平之各類器材入場。
- 試題及答案卷（卡）請務必繳回，未繳回者該科成績以零分計算。
- 試題採雙面列印，考生應注意試題頁數確實作答。
- 違規者依本校招生考試試場規則及違規處理辦法處理。

國立中山大學113學年度碩士班暨碩士在職專班招生考試試題

科目名稱：計算機結構【電機系碩士班己組】　　題號：431007

※本科目依簡章規定「可以」使用計算機（廠牌、功能不拘）（問答申論題）　　

1. **[20%]** In hardware, SYS-1 system has a CPU with a base CPI of X, where X is larger than zero, assuming all references hit in the primary cache (L1) and a CPU clock rate of 2GHz. Assume that the main memory access time is 160 ns, including all the cache miss handling. Suppose the miss rate per instruction at L1 is 5%. Based on the construction of SYS-1 system, there are two systems shown as follows.

   (i) SYS-2 system includes SYS-1 and an additional secondary cache (L2). The access time of L2 is 28 ns for either a hit or a miss. Suppose the miss rate per instruction at L2 is Y, where 0 < Y < 1.

   (ii) SYS-3 system includes SYS-2 and an additional tertiary cache (L3). The access time of L3 is 44 ns for either a hit or a miss. Suppose the miss rate per instruction at L3 is 0.1%.

   We know that SYS-2 system is faster than SYS-1 system by 2 times. In addition, SYS-3 system is faster than SYS-2 system by 1.25 times. Please answer the following questions.

   (a) **(4%)** As regards SYS-1 system, please calculate the memory-stall cycles per instruction.

   (b) **(6%)** Please calculate X.

   (c) **(6%)** Please calculate Y.

   (d) **(4%)** According to the result calculated in (b), the program has three different instruction categories, such as A, B, and C. We know that CPI for A, B, and C is 3, 5, and 6, respectively. The instruction count of A and B is 48 and 30, respectively. Please calculate the instruction count of C.

2. **[10%]** A program, SVM, has the total execution time of 500 ns and can be well-divided into P1 - P4 parts. P1 - P3 can be modified to increase or decrease the individual execution time by the certain approaches. But P4 still keeps identical without any influence. The execution time of P1 - P4 is denoted as T1 - T4, respectively. Assume that T1 - T4 originally are 144 ns, 108 ns, 120 ns, and 128 ns, respectively. There are three different design scenarios as follows.

   ✧ *Design scenario 1: If T1 and T2 are improved by X and Z times, respectively, T3 is increased to 1.34 times accordingly. The corresponding total execution time is decreased to 476 ns.*

   ✧ *Design scenario 2: If T1 and T3 are improved by Y and Z times, respectively, T2 is increased to 1.5 times accordingly. The corresponding total execution time is decreased to 490 ns.*

   ✧ *Design scenario 3: If T2 and T3 are improved by Y and X times, respectively, T1 is increased to 1.375 times accordingly. The corresponding total execution time is increased to 512 ns.*

   Which one is the possible solution of (X, Y, Z)? _____ (***single choice***)

(A) (1.25, 1.5, 1.4)	(B) (1.25, 1.2, 1.75)	(C) (1.4, 1.2, 1.25)	(D) (1.25, 1.5, 1.6)
(E) (1.5, 1.2, 1.25)	(F) (1.4, 1.2, 1.5)	(G) (1.75, 1.4, 1.5)	(H) (1.25, 1.2, 1.25)
(I) (1.25, 1.5, 1.25)	(J) (1.4, 1.75, 1.5)	(K) (1.25, 1.2, 1.5)	(L) (1.4, 1.6, 1.5)

3. **[25%]** Assume that X1 – X7 and Y1 – Y7 are well-represented as the 32-bit single-precision format in IEEE-754 standard as shown in **TABLE I**. We know that the relationship is calculated as follows, $W1 = X1 \times Y1, W2 = X2 \times Y2, \ldots\ldots, W7 = X7 \times Y7$. Please answer the following questions.

(a) **(2%)** If $10^n \leq X5 \leq 10^{n+1}$, where $n \in Z$, please find out the value of n.

(b) **(2%)** If $-10^m \leq Y2 \leq -10^{m-1}$, where $m \in Z$, please find out the value of m.

(c) **(21%)** Please sort these seven numbers (W1 – W7) in descending order.

TABLE I

	Bit 31																								Bit 0
X1	1	0	0	0	0	0	1	1	0	1	1	0	0	1	1	0	0	0	1	0	0	0	0	0	0
Y1	0	1	1	0	0	0	1	0	1	0	1	1	0	1	0	0	1	1	1	1	1	0	0	0	0
X2	0	0	0	1	0	0	1	1	1	0	1	0	1	1	1	0	1	1	0	0	1	0	0	0	0
Y2	1	1	0	1	0	0	0	1	0	0	0	1	0	0	1	0	0	0	1	1	0	0	0	0	0
X3	0	0	1	1	0	1	0	1	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0
Y3	1	0	1	0	1	1	1	0	1	0	1	0	1	0	0	1	1	1	0	0	0	0	0	0	0
X4	1	1	0	1	1	1	0	0	1	1	0	1	1	0	0	0	1	0	0	1	0	0	0	0	0
Y4	0	0	0	0	1	0	0	1	0	0	0	1	1	1	1	1	1	0	1	0	1	0	0	0	0
X5	0	0	0	1	1	1	1	0	0	0	1	0	1	1	0	0	0	1	1	0	0	0	0	0	0
Y5	1	1	0	0	0	1	0	1	1	0	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0
X6	1	1	0	0	1	1	0	0	1	1	1	0	1	1	1	1	0	0	0	1	1	0	0	0	0
Y6	1	0	0	1	0	1	1	0	0	0	1	1	1	1	1	1	0	1	1	0	0	0	0	0	0
X7	0	0	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0
Y7	0	1	0	0	0	1	0	0	0	0	0	1	1	1	1	0	1	0	1	0	1	0	0	0	0

4. **[20%]** The following mathematical equation shows the relationship among different elements in the array, A[ ]. After executing the MIPS codes listed in **Figure 1**, the value of A[i+S] can be computed based on A[i] – A[i+3], where i and S are two positive integers. C0 – C3 denote four integer coefficients. We know that the base address of A[ ] is stored in **$s0**. Please answer the following questions.

(a) **(8%)** Please calculate C0, C1, C2, and C3.

(b) **(4%)** Please calculate i and S.

(c) **(3%)** Please calculate the value of A[i+S] while (A[i], A[i+1], A[i+2], A[i+3]) = (-8, 10, -11, 7).

(d) **(5%)** In hardware implementation, we can utilize 5-stage pipelined MIPS CPU to execute this program. If considering the forwarding (bypass) technique to fix or relax the possible data hazard, what is the minimum number of total clock cycles to complete this program?

$$A[i+S] = C0*A[i] + C1*A[i+1] + C2*A[i+2] + C3*A[i+3] - 5$$

```
0x200   lw  $a0, 128 ($s0)
        lw  $a1, 132 ($s0)
        sub $t0, $a0, $a1
        lw  $a2, 136 ($s0)
0x210   add $t1, $a2, $a2
        sub $t1, $t1, $a1
        add $t2, $t1, $t1
        add $t2, $t2, $t0
0x220   sll $t2, $t2, 3
        sub $t2, $t2, $a0
        lw  $a3, 140 ($s0)
        sll $t0, $a3, 2
0x230   sub $t0, $t0, $a3
        add $t2, $t2, $t0
        sub $t1, $t2, $t1
        addi $t2, $t1, -5
0x240   sw  $t2, 264 ($s0)
```

Figure 1

5. **[15%]** Assume that a dedicated memory system has the parameters as shown below. Please answer the following questions.
   - ✧ *36-bit physical address*
   - ✧ *Cache (virtually-addressed but physically-tagged): direct-mapped, 16KB, 128-bit block size*
   - ✧ *TLB: fully associative, 64 entries*
   - ✧ *Virtual Memory: 42-bit virtual address, 32KB page*

   (a) **(5%)** How many bits are needed in each tag field of this cache?

   (b) **(5%)** How many bits are needed in each tag field of the TLB?

   (c) **(5%)** If each entry of the TLB has three additional status bits, such as Valid bit, Used bit, and Dirty bit, please calculate the total size of the TLB in terms of bytes.

6. **[10%] Figure 2** shows a simple program based on the MIPS codes. Assume that **$s3** = 25, **$s4** = 31, **$s5** = 19, and **$s6** = 21. If **$s0** > 0, **$s1** > 0, and **$s2** > 0, please find out all the possible values of **$s0**.

```
0x1000  div $s0, $s1
        mfhi $s5
        mflo $s3
        div $s0, $s2
0x1010  mfhi $s6
        mflo $s4
```

Figure 2