國立中山大學113學年度
碩士班暨碩士在職專班招生考試試題

科目名稱：電子學(甲組)【電機系碩士班甲組】

—作答注意事項—

考試時間：100分鐘

- **考試開始鈴響前不得翻閱試題，並不得書寫、劃記、作答。**請先檢查答案卷（卡）之應考證號碼、桌角號碼、應試科目是否正確，如有不同立即請監試人員處理。
- **答案卷限用藍、黑色筆(含鉛筆)書寫、繪圖或標示**，可攜帶橡皮擦、無色透明無文字墊板、尺規、修正液（帶）、手錶(未附計算器者)。每人每節限使用一份答案卷，請衡酌作答。
- 答案卡請以2B鉛筆劃記，不可使用修正液（帶）塗改，未使用2B鉛筆、劃記太輕或污損致光學閱讀機無法辨識答案者，後果由考生自負。
- 答案卷（卡）應保持清潔完整，不得折疊、破壞或塗改應考證號碼及條碼，亦不得書寫考生姓名、應考證號碼或與答案無關之任何文字或符號。
- 可否使用計算機請依試題資訊內標註為準，如「可以」使用，廠牌、功能不拘，唯不得攜帶書籍、紙張（應考證不得做計算紙書寫）、具有通訊、記憶、傳輸或收發等功能之相關電子產品或其他有礙試場安寧、考試公平之各類器材入場。
- **試題及答案卷（卡）請務必繳回，未繳回者該科成績以零分計算。**
- **試題採雙面列印，考生應注意試題頁數確實作答。**
- **違規者依本校招生考試試場規則及違規處理辦法處理。**

國立中山大學113學年度碩士班暨碩士在職專班招生考試試題

科目名稱：電子學(甲組)【電機系碩士班甲組】　　題號：431009

※本科目依簡章規定「可以」使用計算機（廠牌、功能不拘）(問答申論題)　　共1頁第1頁

1. (10%) (a) Describe the Early effect in MOSFETs and explain its occurrence mechanism (5%). (b) Define depletion-mode MOSFETs and highlight the distinctions from enhancement-mode MOSFETs (5%).

2. (20%) A full-wave bridge-rectifier circuit with a 1-kΩ load operates from a 120 V (rms) 60 Hz household supply through a 12-to-1 step down transformer having a single secondary winding. It uses four diodes as shown in Figure 1, each of which can be modeled to have a 0.7 V drop for any current.
(a) What is the peak value of the rectified voltage across the load (5%)?
(b) For what fraction of a cycle does each diode conduct (5%)?
(c) What is the peak inverse voltage of each diode (5%)?
(d) If the ripple voltage is to be smaller than 0.3 V, determine the required value of the filter capacitor in parallel with the load resistance (5%).

3. (20%) The NMOS and PMOS transistors in the circuit of Figure 2 are matched with $k_n=k_p=1$ mA/V^2 and $V_{tn}=|V_{tp}|=1$ V. Please find i_{DN} and i_{DP} for (a) $v_I=5$ V (10%) and (b) $v_I=2.5$ V (10%).

4. (30%) Figure 3 shows a three-stage amplifier in which the stages are directly coupled. For our purposes here, we shall assume that the capacitors are large enough to act as perfect short circuits at all signal frequencies of interest. Thermal voltage V_T is 25 mV.
(a) Find the dc collector current in each of the three transistors. Assume $|V_{BE}|\approx 0.7$ V (forward bias), $\beta=100$, and neglect the Early effect (15%).
(b) Find the input resistance R_{in} and the output resistance R_{out} (10%).
(c) Evaluate the voltage gain v_o/v_i (5%).

5. (20%) The transistors in the circuit of Figure 4 have $\beta=100$, Early voltage $V_A=100$ V, and $C_\mu=0.2$ pF. At a bias current of 0.1 mA, $f_T=200$ MHz. Thermal voltage V_T is 25 mV. Find an estimate of the upper 3-dB frequency f_H by the method of open-circuit time constants (list each time constant).

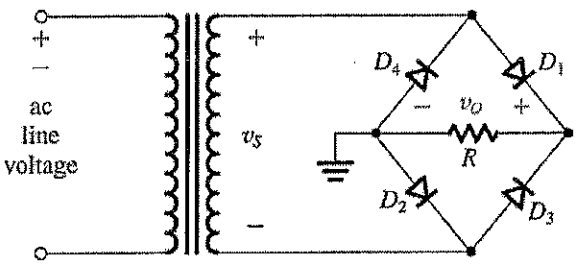

Figure 1

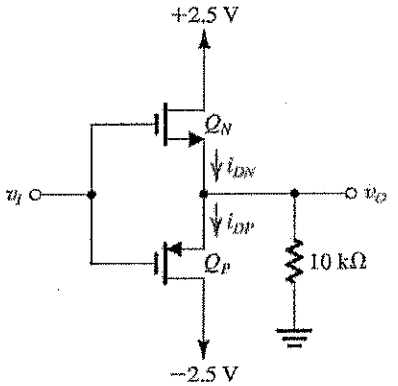

Figure 2

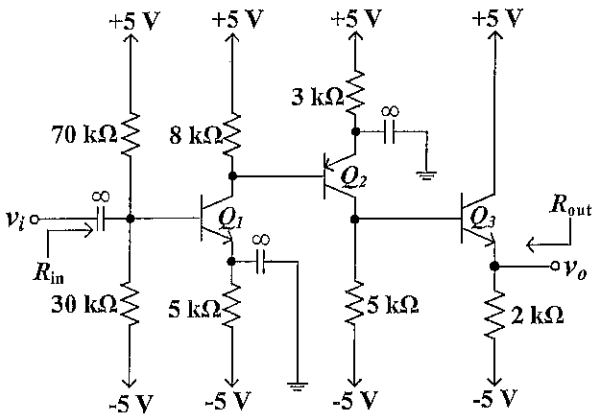

Figure 3

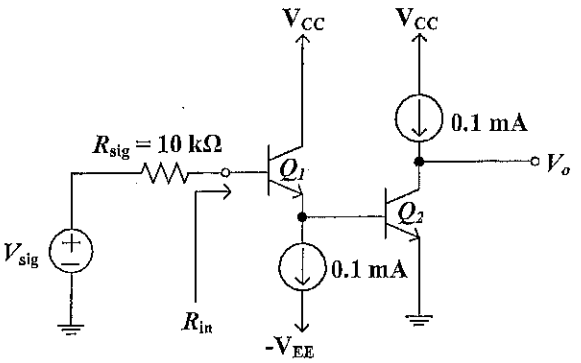

Figure 4

試題請隨卷繳回，請留意背面是否有題