國立成功大學

112學年度碩士班招生考試試題

編　號：181、192、199

系　所：電機工程學系
電腦與通信工程研究所
電機資訊學院-微電、奈米聯招

科　目：電子學

日　期：0206

節　次：第 1 節

備　註：可使用計算機

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※ 考生請注意：本試題可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. (選擇題，每小題 5 分) Please choose the most appropriate answer for the following questions:

(1) The Bode Plot for an open loop gain $A(f)$ of an amplifier is shown in Fig. 1a. The amplifier is used with negative feedback and its DC closed-loop gain is 1,000. What is the gain margin of this amplifier with feedback?

(a) 0 dB, (b) 20 dB, (c) 40 dB, (d) 60 dB.

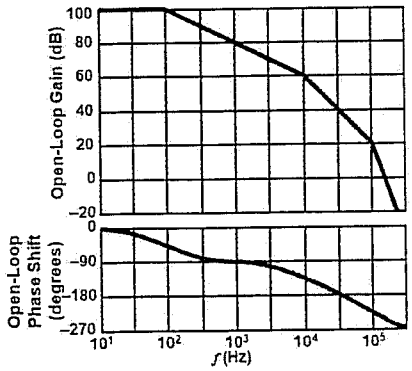

Fig. 1a

(2) Follow (1), what is the phase margin of this amplifier with feedback.

(a) −60°, (b) 45°, (c) 60°, (d) 135°.

(3) What is the value of the low-frequency power-supply rejection ratio with respect to V_{DD} ($PSRR^+ \equiv A_d / A^+$) for a well-matched two stage CMOS op amp shown in Fig. 1b, where g_m and r_o is the transconductance and output resistance of a MOSFET, respectively?

(a) 0, (b) $\approx g_m r_o$, (c) $\approx (g_m r_o)^2$, (d) ∞.

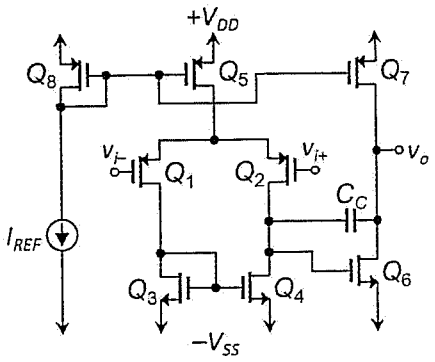

Fig. 1b

(4) Follow (3), what is the value of the low-frequency power-supply rejection ratio with respect to V_{SS} ($PSRR^- \equiv A_d / A^-$)?

(a) 0, (b) $\approx g_m r_o$, (c) $\approx (g_m r_o)^2$, (d) ∞.

(5) Which of the following properties is wrong while applying negative feedback to an open-loop amplifier?

(a) Extends the 3db bandwidth

(b) Improves gain stability

(c) Increases gain-bandwidth product

(d) Reduces nonlinear distortion

(6) For enhancing the high-frequency performance (such as slew-rate and unit-gain frequency) of a two-stage CMOS op amp, we should?

(a) use smaller L for transistors, and operate transistors at larger overdrive voltage,

(b) use smaller L for transistors, and operate transistors at smaller overdrive voltage,

(c) use larger L for transistors, and operate transistors at larger overdrive voltage,

(d) use larger L for transistors, and operate transistors at smaller overdrive voltage,

(7) What is the equivalent impedance of a LC resonator when the inductor (with inductance L) and capacitor (with capacitance C) are connected in **series** and resonate at a frequency of $\omega = 1/\sqrt{LC}$?

(a) 0, (b) C/L, (c) L/C, (d) ∞.

(8) The response of a second-order low-pass filter will be maximally flat for a Q factor equal to

(a) $\sqrt{2}$, (b) 1, (c) $1/\sqrt{2}$, (d) 1/2.

(9) Fig. 1c shows the output response of a single-time-constant (STC) low-pass circuit to a 10-V step input. Please find the time taken, in terms of the time constant τ, for the output to reach 9.9 V.

(a) 0.69τ, (b) 2.2τ, (c) 3.3τ, (d) 4.6τ.

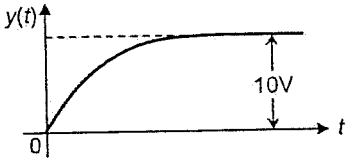

Fig. 1c

(10) What is the output resistance (R_{out}) of the Wilson current mirror shown in Fig. 1d, where g_{mi} and r_{oi} is the transconductance and output resistance of the MOSFET Q_i, respectively?

(a) $r_{o3} + r_{o1}$,

(b) $r_{o3} + (1/g_{m1})$,

(c) $r_{o3} + g_{m3}r_{o3}(1/g_{m1})$,

(d) $r_{o3} + g_{m3}r_{o3}(r_{o2})$

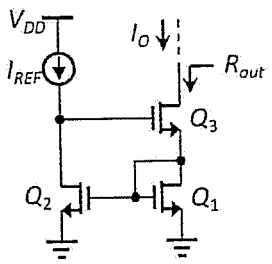

Fig. 1d

2. Fig. 2 considers the use of an op amp with unity-gain frequency of 20 MHz (f_t = 20 MHz), slew rate of 10 V/μs (SR = 10 V/μs), and V_{omax} = 10V in the design of a noninverting amplifier with a nominal gain of 10. Assume $V_{in} = V_i \sin 2\pi ft$.

(a) If V_i = 0.5 V, what is the maximum frequency (f_{max}) before the output distorts? (4%)

(b) If f = 200 kHz, what is the maximum value of V_i (V_{imax}) before the output distorts? (4%)

(c) If V_i = 0.5 mV, what is the useful frequency range of operation (f_{3dB})? (4%)

(d) If f = 50kHz, what is the useful input voltage range (v_i)? (4%)

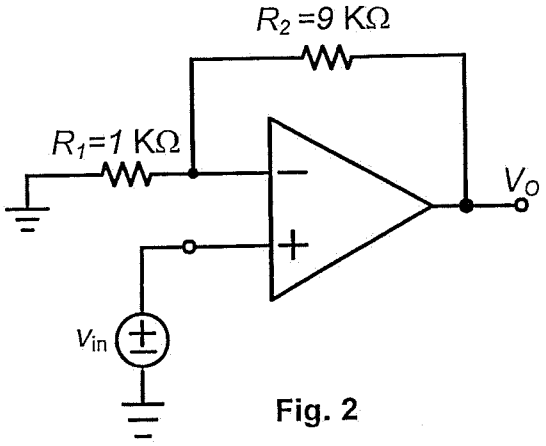

Fig. 2

3. The feedback amplifier of Fig. 3 consists of a common-gate amplifier formed by Q_1 and R_D, and a feedback circuit formed by the capacitive divider (C_1 and C_2) and the common-source transistor Q_f. Neglect r_o and the loading effect of C_1 and C_2 on the basic amplifier. Assume g_m = 5 mA/V, R_D = 10 kΩ, C_1 = 0.9 pF and C_2 = 0.1 pF, and g_{mf} = 2 mA/V.

(a) Find the voltage gain $A_f = V_o/I_s$ (4%)

(b) Find the input resistance (R_{in}) and output resistance (R_{out}) (10%)

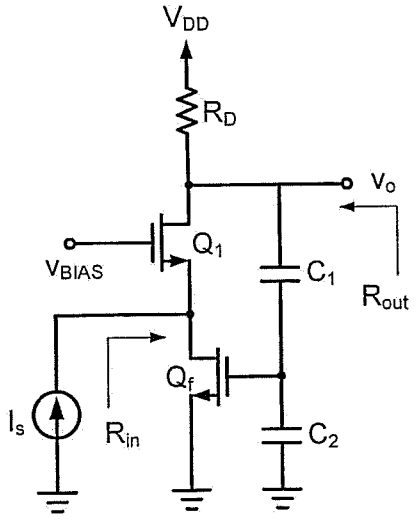

Fig. 3

4. The MOSFET in the circuit of Fig. 4 has threshold voltage V_{tn} = 0.8 V, $k_n = \mu_n C_{ox}(W/L)$ = 5 mA/V^2, R_G = 10 MΩ, and Early voltage V_A = 40 V
   (a) Find the values of R_S and R_D, so that I_D = 0.4 mA, the largest possible value for R_D is used while a maximum signal swing at the drain of ±0.8 V is possible. Neglect the Early effect. (4%)
   (b) Find the value of transconductance (g_m) and output resistance (r_o) of Q_1 at the bias point. (4%)
   (c) If the terminal Z is grounded, terminal X is connected to a signal source having a resistance of 1 MΩ, and terminal Y is connected to a load resistance of 10 kΩ, find the voltage gain from signal source to load. (4%)
   (d) If terminal Y is grounded, find the voltage gain from X to Z with Z open-circuited. What is the output resistance of the source follower? (4%)
   (e) If terminal X is grounded and terminal Z is connected to a current source delivering a signal current of 50 μA, and having a resistance of 100 kΩ, find the voltage signal that can be measured at Y. For simplicity, neglect the effect of r_o. (4%)

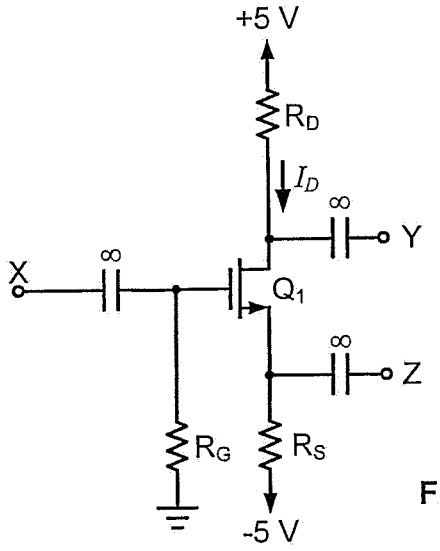

Fig. 4