國立台灣科技大學一百學年度碩士班招生試題

系所組別： 電機工程系碩士班丁一組

科　　目： 數位邏輯

(總分為100分)

1. Please convert the following decimal numbers to binary numbers
   (a) 911 (2%)
   (b) 0.171875 (4%)
   (c) 100.1484375 (4%)

2. Please simplify the following Boolean function in (a) sum of products (5%) and (b) product of sums (5%).

$$F(A,B,C,D) = \sum(1,3,4,6,14)$$

3. A one's complement number system can be used to represent negative numbers as well as positive numbers. Please design a 4-bit one's complement subtraction circuit; i.e., design a circuit that can calculate $O = X - Y$ where O, X, and Y are 4-bit one's complement numbers. The overflow detector should be included in your design. Note that a 4-bit one's complement number is in the range of [–7, 7]. The logic cells allowed in your design are: NOT, NAND, NOR, AND, OR, XOR, XNOR, HA (half adder), and FA (full adder) cells. (15%)

4. Please derive a Boolean function for an odd-parity generator for 6 input data bits in sum-of-product form; i.e., derive a sum-of-product Boolean expression for $P = A \oplus B \oplus C \oplus D \oplus E \oplus F$. (15%)

5. (a) Describe the meaning of *clock skew* and its effect on the maximum clock frequency of a sequential circuit. (5%)
   (b) Describe the meaning of *false path* and give at least two examples. (5%)
   (c) Describe the meaning of *setup time* and its effect on the maximum clock frequency of a sequential circuit. (5%)

6. (a) Construct a T flip-flop with an exclusive-OR gate and a D flip-flop. (4%)
   (b) Draw the block diagrams of Mealy and Moore state machines and describe their differences. (6%)

7. Describe the roles of *state assignment* and *state reduction* when perform logic optimization for a sequential circuit. Give an example to explain. (10%)

8. Design a sequential circuit with two D flip-flops A and B and one input X. When $X = 1$, the state of the circuit remains the same. When $X = 0$, the circuit goes through the state transition from 00 to 10 to 11 to 01, back to 00, and then repeats. You should first derive the state table and state diagram for the circuit and then draw the optimized logic diagram (15%)