國立中正大學
112學年度碩士班招生考試
試 題

[第3節]

科目名稱	計算機系統
系所組別	資訊工程學系-甲組

一作答注意事項一

※作答前請先核對「試題」、「試卷」與「准考證」之系所組別、科目名稱是否相符。

1. 預備鈴響時即可入場，但至考試開始鈴響前，不得翻閱試題，並不得書寫、畫記、作答。
2. 考試開始鈴響時，即可開始作答；考試結束鈴響畢，應即停止作答。
3. 入場後於考試開始40分鐘內不得離場。
4. 全部答題均須在試卷（答案卷）作答區內完成。
5. 試卷作答限用藍色或黑色筆（含鉛筆）書寫。
6. 試題須隨試卷繳還。

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科目名稱：計算機系統　　本科目共 4 頁　第 1 頁

系所組別：資訊工程學系-甲組

I. 單一選擇題：每題5分。

1. Consider the following situation, each CPU or I/O burst in a process happens sequentially from left to right. Which process will be run at timing 23 by using the optimal scheduling algorithm for achieving the smallest average waiting time?

   (a) P1

   (b) P2

   (c) P3

   (d) P4

   (e) P5

	CPU Burst	I/O Burst	CPU burst	I/O burst	CPU burst	Arrival time
P1	3	6	3			5
P2	5	0	5	0	5	2
P3	5	2	5	2	5	0
P4	3	4	8			2
P5	1	2	4			7

2. Unified virtual memory uses _____ to cache both process page and file data.

   (a) page cache

   (b) double cache

   (c) buffer cache

   (d) disk block cache

   (e) CPU cache

3. Which of the following is true? Here "MIPS" means million instructions per second.

   (a) For two programs, their MIPSs are the same while they are executed on the same computer.

   (b) MIPS is a good metric to measure performance.

   (c) Two programs running the same machine have the same MIPS.

   (d) Relative MIPS cannot reflect the execution time of a program.

   (e) MIPS can represent the execution time of a program on a given machine.

4. Which of the following is true?

   (a) Floating-point addition is associative.

   (b) Right shift instruction is the same as integer division by a power of 2.

   (c) The hardware of multiplication and division can be the same.

   (d) Booth's algorithm is used to addition.

   (e) Overflow occurs while adding two positive numbers and the sum is negative.

5. Which of the following is false, where RISC and CISC stand for "reduced instruction set computer" and "complex instruction set computer"?

   (a) RISC has fewer instructions than CISC.

   (b) RISC has fewer addressing modes than CISC.

(c) CISC always has better performance than RISC.

(d) RISC is suitable for mobile devices.

(e) CISC always consumes much power than RISC.

II. 多重選擇題：所有答案必須符合才算分，每題 5 分。

1. Which of the following statements are incorrect?

(a) Filenames are usually stored in directory files.

(b) Mounting points are usually regular files.

(c) The technique used to improve I/O efficiency by temporarily storing repeatedly-used data is called buffering.

(d) DMA controller are efficient for large I/O requirements.

(e) Modern operating system usually knows the geometry of disks.

2. Which of the following terms is a hardware-based synchronization tool?

(a) CAS instruction

(b) Peterson's Solution

(c) DMA

(d) Banker's algorithms

(e) MMU

3. Which of the following situation must induce the context switch?

(a) When a process is complete.

(b) When an interrupt occurs.

(c) When the state of a process moves from waiting to running.

(d) When the state of a process moves from running to waiting.

(e) When a system call is being called.

4. A pipelining consists of five stages: IF (Instruction Fectching), ID (Instruction Decoding), Exe (Execution), Mem (Memory), and WB (Write Back). For the following code shown in Figure 1, what types of dependencies or hazards are there in this code?

```
lw   $1,  10($0)
lw   $2,  20($0)
add $3,   $2, $4,
lw   $1,  30($0)
lw   $1,  40($0)
```

Figure 1

(a) Structural hazard

(b) Data hazard

(c) Data dependency

(d) Output dependency

(e) Control hazard

5. What techniques can be applied to solve the hazards in Figure 1?
   (a) Forwarding
   (b) Code interchanging
   (c) Delayed branch
   (d) Register renaming
   (e) Loop unrolling

III. 填空題：不需要做答過程，每個答案務必標明題號和空格編號，每個空格 5 分。

1. In the past, disks in IBM PC are addressed by 24-bit CHS address, where 10 bits for cylinders(C), 8 bits for disk heads(H), and 6 bits for sectors(S). Assuming the capacity of a sector is 512 bytes. The largest capacity of the disk is __(a)__ Byte. Consider the following disk I/O request sequence (assume the requests are represented by CHS address by hexadecimal, and the disk has the maximum capacity with the above addressing manner)1AC320, A2F5BC, 7A182D, EF6714, F0D76, C0F1D1, FF2236. The seek distance is __(b)__ (cylinder) when using the C-SCAN scheduling algorithm (please answer a decimal number).
2. The following code section is retrieved from Linux kernel code (/mm/filemap.c), and it describes the rules of locking order. The main purpose of predefining the lock order is to break which deadlock

```
/*
 * Lock ordering:
 *  ->i_mmap_rwsem        (truncate_pagecache)
 *    ->private_lock      (__free_pte->block_dirty_folio)
 *      ->swap_lock
 *
 *  ->i_rwsem
 *    ->invalidate_lock             (acquired by fs in truncate path)
 *
 *  ->mmap_lock
 *    ->i_mmap_rwsem
 *      ->page_table_lock or pte_lock (various, mainly in memory.c)
 *
 *  ->mmap_lock
 *    ->invalidate_lock             (filemap_fault)
 *
```

condition for preventing deadlock? __(c)__.

	Allocation				Max Required					
	A	B	C	D	A	B	C	D		
T_0	1	2	0	2	4	3	3	7		
T_1	0	1	1	2	2	4	2	4		
T_2	1	2	4	0	3	6	5	1		
T_3	1	2	0	1	2	3	2	3		
T_4	1	0	0	1	3	1	1	2		

3. Consider the above snapshot of a system: Suppose there are 5 tasks (T0 through T4) and 4 different resource types (A, B, C, D). Assume Resources (A, B, C, D) have (6, 7, 6, 10) instances, respectively. (i.e., A has 6 instances, B has 7 instances, C has 6 instances, and D has 10 instances). What is the maximum number of Resources (A, B, C, D) that the OS can grant T0 to request immediately? __(d)__.
4. __(e)__ is a technology used to address the performance and reliability issues of the storage system by using multiple disks.
5. The decimal value for the IEEE 754 single-precision representation of the number 1, 01111110, 11000000000000000 is __(f)__.
6. Assume an instruction cache miss rate for a program is 3% and a data cache miss rate is 5%. Assume a processor has a CPI of 2 without any stalls, the miss penalty is 100 cycles for all misses, and the percent of accessing data cache is 35%. The sppedup is __(g)__ while a processor with a perfect cache that never missed run compared with the previous one.
7. Given a 5GHz machine with a CPI of 1.0, we assume the miss rate of the cache is 2%, the access time of DRAM is 100ns. The average memory time is __(h)__. If we add a L2 cache with 5ns access time and decrease of overall main memory miss rate to 0.5%, the average memory time is __(i)__.
8. Suppose you want to perform two sums: one is a sum of two scalar variables and one is a matrix sum of a pair of two-dimensional arrays, size 1000 by 1000. The speedup is __(j)__ if you use 1000 processors to do them.