國立中正大學
112學年度碩士班招生考試
試 題

[第2節]

科目名稱	電子學
系所組別	電機工程學系－電磁晶片組 計算機工程組 晶片系統組

－作答注意事項－

※作答前請先核對「試題」、「試卷」與「准考證」之系所組別、科目名稱是否相符。

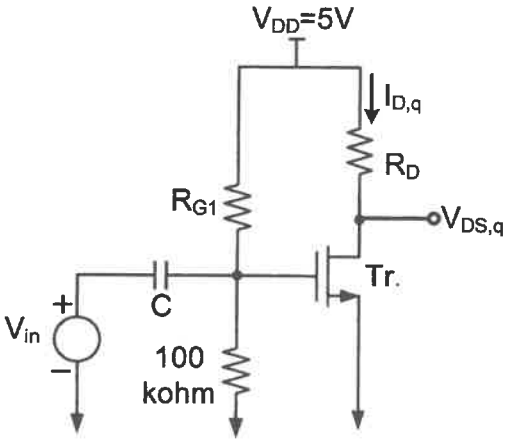
1. 預備鈴響時即可入場，但至考試開始鈴響前，不得翻閱試題，並不得書寫、畫記、作答。
2. 考試開始鈴響時，即可開始作答；考試結束鈴響畢，應即停止作答。
3. 入場後於考試開始40分鐘內不得離場。
4. 全部答題均須在試卷（答案卷）作答區內完成。
5. 試卷作答限用藍色或黑色筆（含鉛筆）書寫。
6. 試題須隨試卷繳還。

國立中正大學 112 學年度碩士班招生考試試題

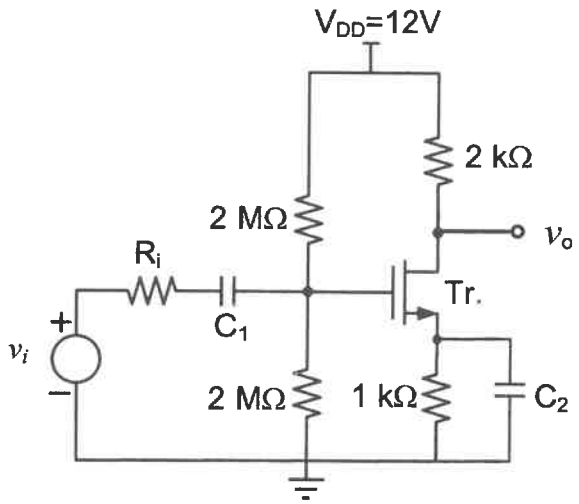
科目名稱：電子學　　本科目共 4 頁　第 1 頁

系所組別：電機工程學系-電磁晶片組、計算機工程組、晶片系統組

1. (10%) In the following circuit, the transistor Tr. operates with V_T=0.5 V, $\mu_n C_{OX} W/2L$=0.2 mA/V^2, and no channel length modulation effect should be considered.
   Please properly choose (a) (5%) R_D and (b) (5%) R_{G1} to let the mid-band voltage gain become −4 as $V_{DS,q}$ being 2 V

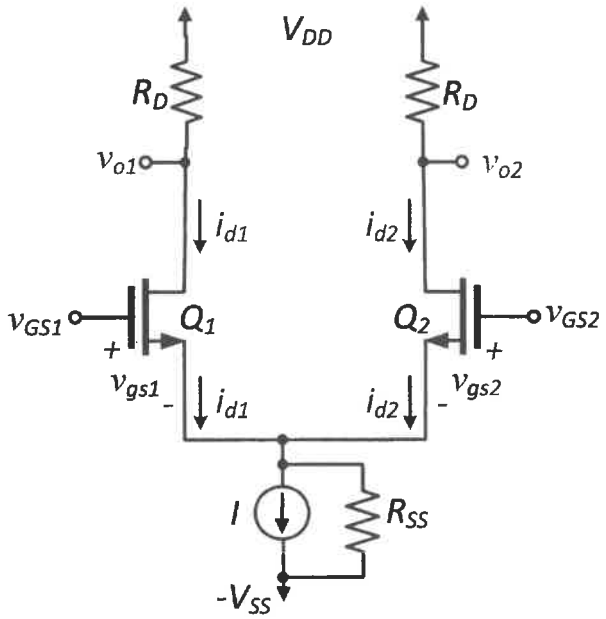


2. (15%) For a common-source MOSFET amplifier, the transistor Tr. has V_T = 1V, $\mu_n C_{OX} W/L$== 0.2 mA/V^2, C_{gs}= 3 pF, C_{gd}= 2.5 pF and V_A= 20 V, and no channel length modulation effect should be considered. Both of coupling capacitors (C_1 and C_2) are large enough to be short circuits at high frequency
   (a) (5%) What is the 3dB bandwidth if R_i= 0
   (b) (5%) Find the 3dB bandwidth if R_i=10 kΩ.
   (c) (5%) What kind of roles are played by C_1 and C_2?



3. (25%) A MOS differential amplifier with ±1-V supplies and 1 mW maximum quiescent power dissipation to provide the differential voltage gain A_d of which being 10 V/V .
   (a) (5%)What is the required V_{ov} to support the input differential signal v_{id} (=v_{GS1}- v_{GS2}) being 0.25 V.
   (b) (5%)What's the transconductance of Q_1 and Q_2?
   (c) (5%)Please explain the role of R_D and the limitation to choose its value?
   (d) (5%)Assume k'_n = 500 μA/V^2, to specify the required aspect ratio (W/L) as neglecting the Early effect.

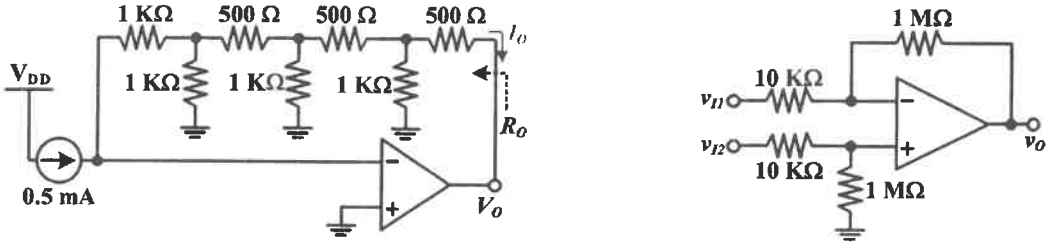
(e) (5%)Please summarize the effects of R_{SS} happened to differential voltage gain A_d and common-mode voltage gain A_{CM}.



4. Fig. P4 shows two applications of op amp. Assuming the op amps used in Fig. P4 are ideal, please answer the following questions:

   (1) Find the I_O and R_O indicated in Fig. P4(a). (5%)

   (2) If the op amp used in Fig. P4(b) has offset voltage (V_{OS}) of 4 mV, input bias current (I_B) of 1 μA, and input offset current (I_{OS}) of 0.1 μA, find the largest dc offset voltage at the output. (10%)



(a)　　(b)

Fig. P4

5. Fig. P5 shows a feedback amplifier, where transistors M_1, M_2, and M_3 are biased at saturation region with a bias current of 0.2 mA and an overdrive voltage of 0.4 V. Meanwhile, each current source is implemented using single transistor so that contributes an output resistance. Assume that $|V_A| = 20$ V for all transistors, please find the close-loop gain (v_o/v_i). (20%)

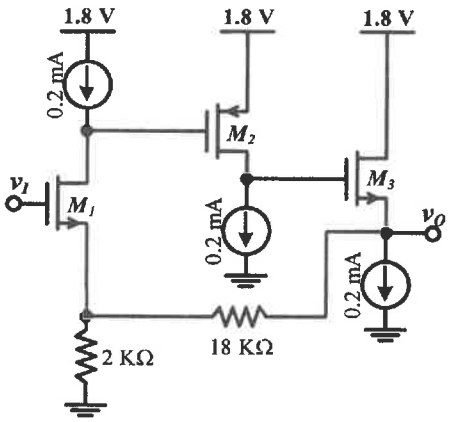


Fig. P5

6. The CMOS logic gate shown in Fig. P6 drives a load capacitance of 10 fF, where the input waveforms are periodic with a cycle time of 1 ns. Please determine the dynamic power dissipation when the logic gate drives the load capacitance with ignoring the short circuit current. (8%)

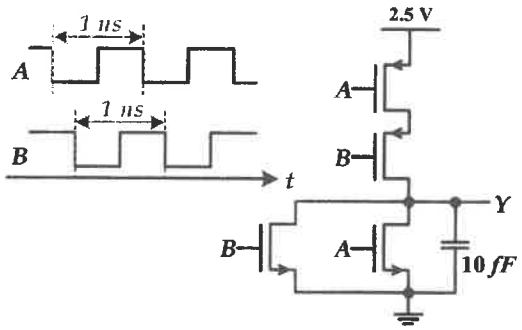


Fig. P6

7. The CMOS inverter shown in Fig. P7 is fabricated using the following parameters: $V_{TH,n} = |V_{TH,p}| = 0.5$ V, $2\mu_p C_{ox} = \mu_n C_{ox} = 100\ \mu A/V^2$, please find the output voltage of V_Y. (7%)

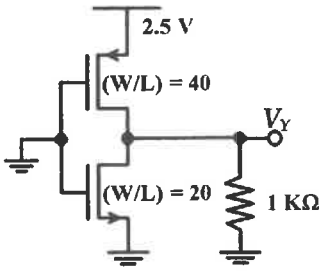


Fig. P7