國立中正大學
112學年度碩士班招生考試
試 題

[第1節]

科目名稱	計算機組織
系所組別	電機工程學系－計算機工程組 晶片系統組

－作答注意事項－

※作答前請先核對「試題」、「試卷」與「准考證」之系所組別、科目名稱是否相符。

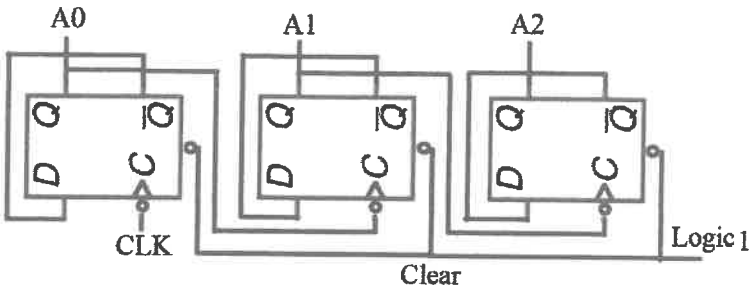
1. 預備鈴響時即可入場，但至考試開始鈴響前，不得翻閱試題，並不得書寫、畫記、作答。
2. 考試開始鈴響時，即可開始作答；考試結束鈴響畢，應即停止作答。
3. 入場後於考試開始40分鐘內不得離場。
4. 全部答題均須在試卷（答案卷）作答區內完成。
5. 試卷作答限用藍色或黑色筆（含鉛筆）書寫。
6. 試題須隨試卷繳還。

國立中正大學 112 學年度碩士班招生考試試題

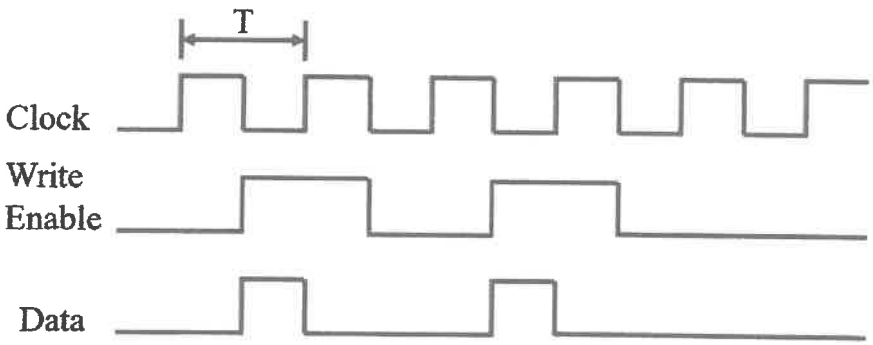
科目名稱：計算機組織　　本科目共 2 頁　第 1 頁

系所組別：電機工程學系-計算機工程組、晶片系統組

1. (20%) An engineer designs a watching dog timer for MIPS platform using D type flip-flops as follows. With the initial condition $(Q,\bar{Q}) = (1,1)$, what are the outputs from A0 to A2 at 5th positive clock edge? Why?



2. (20%) A timing sequence for writing data to the memory is as shown below. Please re-draw a timing sequence with the conditions of (a) memory is triggered by clock's positive edge, (b) write enable is high level triggered, (c) data's hold time is 3/4 T, (d) data's setup time is 1/2 T.



3. (20%) Assume two different CPUs designs running with the same instruction set architecture as shown below. The CPU1 is with a clock rate of 2.5 GHz, and the CPU2 is with a clock rate of 3 GHz. Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D.

   (a). (10%) Please provide the global CPI for each case?

   (b). (10%) What is the clock cycles required for each CPU design?

	CPI for each instruction class			
	A	B	C	D
CPU1 CPI	1	2	3	3
CPU2 CPI	2	2	2	2

4. (20%) Assume the instructions are as follows, and the bne is determined at the output of the register file.
   (a). (10%) Please plot the MIPS five-stage pipeline sequence diagram without forwarding. (10%)
   (b). (10%) Please re-plot the diagram of question (a) with forwarding. (10%)

```
add  $10, $21, $9
lw   $9,  20($10)
bne  $10, $9, 1000
```

5. (20%) Translate the following loop into C. Assume that the C-level integer *i* is held in register $t1, $s2 holds the C-level integer called *result*, and $s0 holds the base address of the integer *MemArray*.

```
        addi  $t1,  $0,    0
LOOP:   lw    $s1,  0 ($s0)
        add   $s2,  $s2,   $s1
        addi  $s0,  $s0,   4
        addi  $t1,  $t1,   1
        slti  $t2,  $t1,   100
        bne   $t2,  $s0,   LOOP
```