國立成功大學

112學年度碩士班招生考試試題

編 號: 158

系 所: 生物醫學工程學系

科 目:電子學

日 期: 0206

節 次:第2節

備 註:可使用計算機

編號: 158

國立成功大學 112 學年度碩士班招生考試試題

系 所:生物醫學工程學系

考試科目:電子學 考試日期:0206,節次:2

第1頁,共2頁

※ 考生請注意:本試題可使用計算機。 請於答案卷(卡)作答,於本試題紙上作答者,不予計分。

- 1. (20%) Please explain the following terminologies:
 - a) depletion region (4%), b) emitter-coupled logic (ECL) (4%), c) emitter resistance (4%), d) frequency response of amplifiers (4%), e) dominant pole (4%).
- 2. (25%) For the circuits shown in Figure 1. Please answer the following questions
 - (a) Please derive the mid-band gain of the circuit (7%)
 - (b) Please derive transfer function in the low-frequency band (8%)
 - (c) Please determine the 3-dB frequency in the high-frequency band (10%)

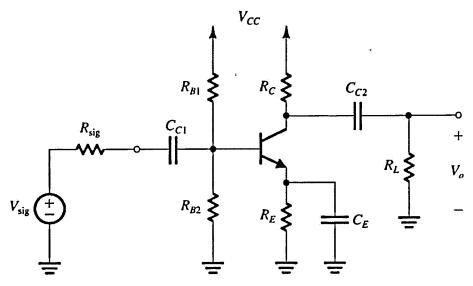


Figure 1

3. (20%) Please derive input resistance (4%), gain (8%), and output resistance (8%) of the circuit shown in Figure 2.

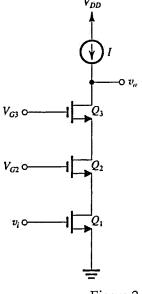


Figure 2

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4. (10%) What is the peak inverse voltage of the circuit shown in Figure 3?

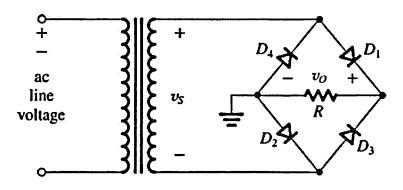


Figure 3

- 5. (25%) Figure 4 shows a discrete-circuit amplifier. The input signal v_{sig} is coupled to the gate through a very large capacitor (shown as infinite). The transistor source is connected to ground at signal frequencies via a very large capacitor (shown as infinite). The output voltage signal that develops at the grain is coupled to a load resistance via a very large capacitor (shown as infinite). All capacitors behave as short circuits for signals and as open circuits for DC.
 - (a) It the transistor has $V_t = 1 \text{ V}$, and $k_n = 4 \text{ mA/V}^2$, verify that the bias circuit establishes $V_{GS} = 1.5 \text{ V}$, $I_D = 0.5 \text{mA}$, and $V_D = +0.7 \text{ V}$. That is, assume these values, and verify that they are consistent with the values of the circuit components and the device parameters. (5%)
 - (b) Find g_m and r_o if $V_A = 100 \text{ V}$. (5%)
 - (c) Draw a complete small-signal equivalent circuit for the amplifier, assuming all capacitors behave as short circuits as signal frequencies. (5%)
 - (d) Find R_{in} , v_{gs}/v_{sig} , v_o/v_{gs} , and v_o/v_{sig} . (10%)

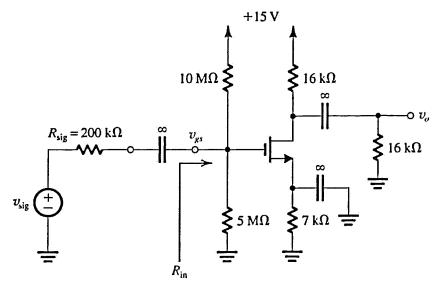


Figure 4