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注意事項：

1、本科目應使用本校提供之電子計算器。

2、請於答案卷上規定之範圍作答，違者該題不予計分。

1.　(a) Fig. 1 is a CMOS logic gate, what is the logic function of out? (5%)

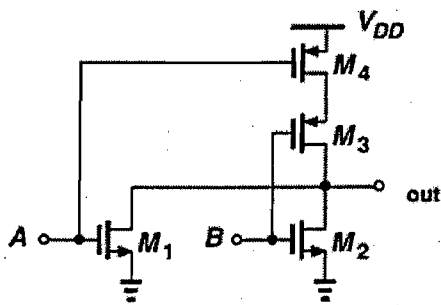　　(b) Please draw a three inputs NAND gate using static CMOS logic gate. (5%)
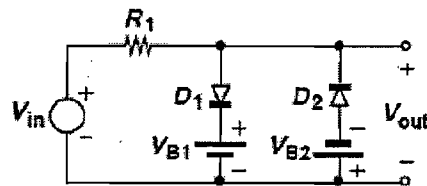

Fig. 1. CMOS logic gate.　　　　　　　Fig. 2. Diode circuit with sin input.

2.　As shown in Fig. 2, the input is a sine wave $V_{in}= 4 \sin(\omega t)$ V,　R_1=2KΩ, diode's turn on voltage of D_1 and D_2 is $V_{D,on}$=0.7 V. V_{B1}= -1V and V_{B2}=2V. Please plot

　(a) the output waveform (Vout v.s. time).　　(10%)

　(b) the voltage transfer curve (Vout v.s. Vin).　　(10%)

3.　Fig. 3 is a common emitter (CE) amplifier. If the current pass R_C is 1mA,　R_C = 1KΩ，β=100 , Early voltage V_A=10 V and temperature at 300°K，please find

(a) g_m (transconductance).　(5%)

(b) Av (voltage gain).　　　(5%)

(c) R_{in}　(input resistance).　　(5%)
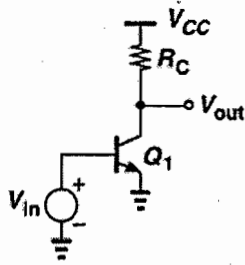
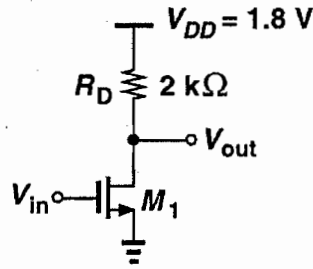(d) R_{out} (output resistance).　　(5%)

Fig. 3. Common Emitter Amplifier.

Fig. 4: Common Source stage.

4. In Fig.4, $u_n C_{ox}$= 100 uA/V^2, V_{TH}=0.4V, W/L=20/0.18 and λ =0.

(a) Find gate voltage (V_{GS}) if I_D=0.5 mA, and verify M_1 operates in saturation. (5%)

(b) Calculate the voltage gain Av. (5%)

(c) Find input resistance R_{in} and output resistance R_{out}. (5%)

(d) Find the maximum R_D if M_1 still in edge of saturation. (5%)

5. Design a full-wave rectifier as shown in Fig. 5 to deliver an average power of 2 W to a cellphone with a voltage of 3.6 V and a ripple of 0.2V ($V_{D,on}$ =0.8V, f_{in}=60 Hz). Find

(a) the required capacitor C_1. (5%)
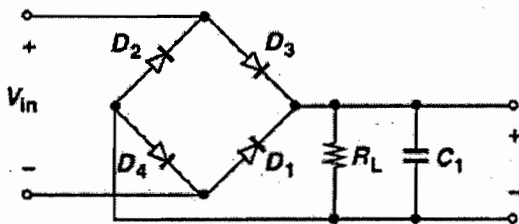
(b) the peak voltage of V_{in}. (5%)

Fig. 5. Full-wave rectifier.

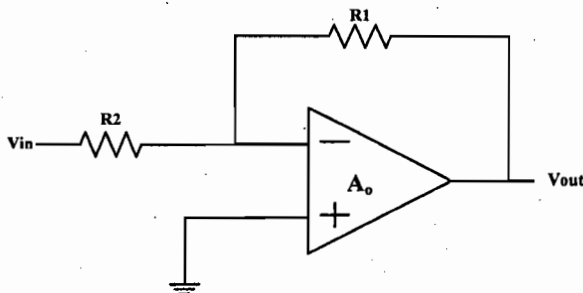6. As shown in Fig. 6, if A_o is not infinite (i.e. the operational amplifier is not ideal), please derive the Vout / Vin ? (20%)

Fig. 6. Operational amplifier.