國立中正大學
111 學年度碩士班招生考試
試 題

[第 3 節]

科目名稱	計算機系統
系所組別	資訊工程學系-甲組

—作答注意事項—

※作答前請先核對「試題」、「試卷」與「准考證」之系所組別、科目名稱是否相符。

1. 預備鈴響時即可入場，但至考試開始鈴響前，不得翻閱試題，並不得書寫、畫記、作答。
2. 考試開始鈴響時，即可開始作答；考試結束鈴響畢，應即停止作答。
3. 入場後於考試開始 40 分鐘內不得離場。
4. 全部答題均須在試卷（答案卷）作答區內完成。
5. 試卷作答限用藍色或黑色筆（含鉛筆）書寫。
6. 試題須隨試卷繳還。

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科目名稱：計算機系統　　本科目共 4 頁　第 1 頁

系所組別：資訊工程學系-甲組

1　選擇題 (2 pt each):

(1) What is a possible reason that applications may not use the hardware instructions provided for locking and unlocking?

A. Because the instructions are privileged
B. Because high level languages don't support them
C. Because they waste CPU cycles
D. Because they are not atomic
E. None of the above is the reason that applications don't use hardware locking.

(2) Shared memory is a very fast mechanism for interprocess communication because both processes can see any changes instantly. What is the main drawback to shared memory?

A. It is limited to a small space.
B. It requires an OS call.
C. It is limited to two processes at one time.
D. It may require synchronization.
E. None of the above is a drawback to shared memory.

(3) What does the UNIX exec system call do?

A. Creates a new empty process.
B. Creates a copy of the parent process.
C. Creates a new process from another program file.
D. Starts a new program running in another process.
E. Starts a new program running in current process.

(4) Which of the following is **NOT** an advantage of using a kernel thread library?

A. Threads can use multiple CPUs.
B. Library calls involve an interrupt.
C. Simplified programming model.
D. Blocking calls do not block entire process.
E. They are not "thread safe".

(5) Which of these did we **NOT** say was a time we could bind source program address to physical memory addresses?

A. Coding
B. Linking
C. Loading into RAM
D. Process execution
E. All of the above are times that addresses can be bound to physical addresses.

(6) What hardware was added to computers to reduce the multiple memory fetch that would have been necessary with memory paging?
A. TLB
B. Page limit register
C. Valid bit
D. Relocation register
E. None of the above hardware options relates to the multiple memory fetch problem.

(7) With paged memory hardware there was a bit in each page table entry called the "valid" bit that originally meant the page was not a part of the logical address space for the process. When Virtual Memory was implemented on top of this hardware we changed the significance of that bit. What did it now mean?
A. The page was not currently in memory.
B. The page had not been referenced lately.
C. The page was read only.
D. The page was part of the kernel space.
E. The page was not a part of the logical address space.

(8) How many page tables are there in a normal single-level paged memory system?
A. One
B. One per thread
C. One per process
D. One per CPU
E. None of the above is the correct number of page tables.

(9) What is the function of a log based file system?
A. Log transactions of file system metadata updates to increase reliability.
B. Log all data writes for security auditing.
C. Log all file opens to limit access to files.
D. Log all data transactions to increase reliability.
E. None of the above

(10) What does message signing accomplish?
A. It verifies the sender.
B. It prevents repudiation of the message.
C. It prevents modification of the message after receipt.
D. Both A and B are true.
E. All of the above are true.

(11) What technique allows us to run multiple operating systems at the same time on the same machine?

A. Interrupt Vectors
B. Virtual Machines
C. Soft Real-Time
D. Network OS
E. Distributed OS

(12) Which of the following mechanisms is **NOT** for increased performance of disk systems?

A. Tagged queuing (native command queuing)
B. Disk (controller) hardware buffering
C. Dynamic Memory Access
D. Sector Sparing
E. All of the above were for increased performance.

(13) What do we call that portion of an OS that is always in the memory after the OS is booted?

A. Shell
B. Command Interface
C. Device Driver
D. Kernel
E. Scheduler

(14) When a program is going to instruct a device controller to do some I/O operation it needs several pieces of information. Which of these is **NOT** a parameter that needs to be passed to a controller for an I/O operation?

A. Memory (buffer) address
B. Interrupt number
C. Device storage address
D. Operation control (type)
E. All of the above are parameters passed to a controller for an I/O operation.

(15) What is the basic principle that allows caching at all levels to increase system performance?

A. The OS can buffer ahead when reading the disk
B. Memory is faster than disks
C. Programs don't access memory randomly -- they have "locality of reference"
D. It eliminates rotational latency
E. None of the above allows caching to work so well.

2 Short Answer (5 pt each): Your answers should be as concise as possible; aim for three to five sentences.

(1) Describe the difference between dynamic loading and dynamic linking.

(2) What is the purpose of processor affinity?

(3) Briefly describe the concept of priority inversion.

(4) Why do applications not use spin-locks? What do they do instead?

3 (5 pt each)

(1) Write down the "CPU performance equation". (Hint: CPU execution time = ? * ? * ?)

(2) A design team adds a "multiply-accumulate" instruction (i.e., Rd += Rs * Rt) to combine separate "multiply" (Rd = Rs*Rt) and "add" (Rd = Rs + Rt) instructions for AI performance. Briefly describe how the parameters in the CPU performance equation can be affected.

4 (5 pt each)

(1) What is a pipeline hazard?

(2) A custom 5-stage processor datapath (i.e., IF/ID/EX/MEM/WB; same in the textbook) has its critical path in the instruction decoder, and the design team plans to pipeline ID into 2 stages (i.e., IF/ID1/ID2/EX/MEM/WB) for better performance. List what additional hazards may occur (show instruction sequences).

5 (5 pt each)

(1) What is BHT?

(2) Use a simple case to illustrate why a 2-bit BHT can have better performance than a 1-bit BHT.

6 (5 pt each) Given the following memory references (word addresses in decimal): 8, 11, 21, 22, 17, 30, 134, 38, 43, 48.

(1) What is the number of misses for a direct-mapped cache with 10 blocks, each of which contains only 1 word? Show the type of each cache miss (i.e., one of 3C).

(2) Repeat (1) if each cache block contains 10 words.

7 (10 pt) List 3 possible technical reasons why Apple wants to develop its own processor SoC (e.g., M1) to replace Intel's CPU for Mac.