(100)輔仁大學碩士班招生考試試題	考試日期：100 年 3 月 18 日第 2 節
	本試題共 7 頁 (本頁為第 1 頁)

科目：邏輯設計　　系所組：電機工程學系丁組

1. Draw the logic circuit of a four-to-one-line multiplexer. (5%)

2. Simplify the following Boolean expression using **algebraic method:**
   A′B(D′+C′D)+ B(A+A′CD) + ABEF. (5%)

3. Use four variables map to simplify the following Boolean function *F*, together with the don't-care *d*. Draw the logic diagram using two-level forms (a) AND-NOR (b) NOR-NOR; (c) NAND-NAND; (d) NOR-OR. (12%) (**Must not attach any inverter at the output**)
   $F(A, B, C, D) = \Sigma m(0, 3, 4, 8, 10, 11)$, $d(A, B, C, D) = \Sigma m(1, 2, 6)$

4. **(a)** How many 32K × 8 RAM chips are needed to provide a memory capacity of 512K bytes? **(b)** How many lines of the address must be used to access 512K bytes? **(c)** How many of these lines are connected to the address inputs of all chips? **(d)** Specify the size of the address decoder needed in the design. (10%)

5. Consider the waveforms of a clock and of an input data signal as shown in Fig. 1. Connect them to (a) a positive level triggered D-latch (b) a positive edge triggered D flip-flop and (c) a negative edge triggered T flip-flop. Draw the output's (Q) waveform, assuming that the initial value of Q is 0. (**clock and input data** 波形也要畫在答案紙上) (6%)

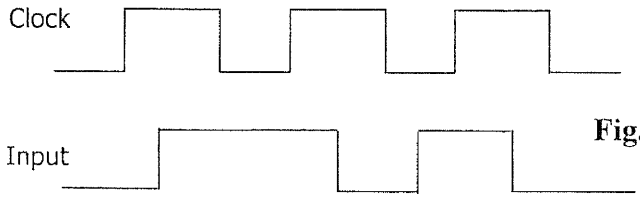

Fig. 1

6. Design a counter with the following repeated binary sequence: 0, 1, 4, 6, 5 using three (1) D flip-flops and (2) JK flip-flops. (15%)

7. A Moore sequential circuit has one input X and one output Y. The output *Y=1* iff the total number of 1's received is odd and divisible by 3, otherwise *Y=0*. (Note that 3, 9, 15 is odd and divisible by 3) (a) Draw the state diagram; (b) Write a behavioral HDL model (Verilog or VHDL) of the machine. (5%, 9%)

8. Assume X being a 3-bit unsigned number. Design a modular squarer circuit that generates X^2 mod 5. (e.g. X= 4, X^2 mod 5 = 1 and X= 2, X^2 mod 5 = 4) (10%)

9. Explain why the registered outputs are generally used in Mealy machine? (5%)

10. Briefly explain the following technical terms (18%)
    (1) static 1-hazard (2) hold time (3) ring counter (4) carry select adder (5) carry save adder (6) essential implicant.

※ 注意：1.考生須在「彌封答案卷」上作答。
2.本試題紙空白部份可當稿紙使用。
3.考生於作答時可否使用計算機、法典、字典或其他資料或工具，以簡章之規定為準。