國立中山大學111學年度
碩士班暨碩士在職專班招生考試試題

科目名稱：計算機結構【電機系碩士班已組】

－作答注意事項－

考試時間：100分鐘

- **考試開始鈴響前不得翻閱試題，並不得書寫、劃記、作答。**請先檢查答案卷（卡）之應考證號碼、桌角號碼、應試科目是否正確，如有不同立即請監試人員處理。
- **答案卷限用藍、黑色筆(含鉛筆)書寫、繪圖或標示**，可攜帶橡皮擦、無色透明無文字墊板、尺規、修正液（帶）、手錶(未附計算器者)。每人每節限使用一份答案卷，請衡酌作答(不得另攜帶紙張)。
- 答案卡請以2B鉛筆劃記，不可使用修正液（帶）塗改，未使用2B鉛筆、劃記太輕或污損致光學閱讀機無法辨識答案者，後果由考生自負。
- 答案卷（卡）應保持清潔完整，不得折疊、破壞或塗改應考證號碼及條碼，亦不得書寫考生姓名、應考證號碼或與答案無關之任何文字或符號。
- 可否使用計算機請依試題資訊內標註為準，如「可以」使用，廠牌、功能不拘，唯不得攜帶具有通訊、記憶或收發等功能或其他有礙試場安寧、考試公平之各類器材、物品（如鬧鈴、行動電話、電子字典等）入場。
- **試題及答案卷（卡）請務必繳回，未繳回者該科成績以零分計算。**
- **試題採雙面列印，考生應注意試題頁數確實作答。**
- **違規者依本校招生考試試場規則及違規處理辦法處理。**

國立中山大學 111 學年度碩士班暨碩士在職專班招生考試試題

科目名稱：計算機結構【電機系碩士班己組】　　題號：431007

※本科目依簡章規定「可以」使用計算機（廠牌、功能不拘）（問答申論題）　

1. **[20%]** (1) **(12%)** Write MIPS assembly codes that implement a **sort** function on an array *v* with the size of *n*. Note that you need to add comments to each line of your written assembly codes (2) **(8%)** Please also describe your ideas on implementing the sort function using a high-level programming language such as C. Note that your written high-level programming codes should support your assembly codes.

2. **[20%]** Explain the following terms.
   (a) **(4%)** Forwarding
   (b) **(4%)** Fully associative cache
   (c) **(4%)** IEEE 754 standard
   (d) **(4%)** Branch prediction
   (e) **(4%)** SRAM

3. **[20%]** The following questions are for the five-pipeline-stage MIPS processor design.
   (a) **(10%)** Draw the **data path** of the five-pipeline-stage MIPS processor with hazard detection and forwarding capabilities.
   (b) **(5%)** Illustrate and explain in details how a branch instruction is executed in your drawn data path of the five-pipeline-stage MIPS processor.
   (c) **(5%)** What is data hazard and how this problem can be resolved in the five-pipeline-stage MIPS processor design in (a)? Please design an example assembly program to help illustrate and explain in details.

4. **[20%]** Cache designs are important for enhancing the performance of a processor system. Below is a list of 32-bit memory address references, given as word addresses.
   75, 33, 131, 18, 217, 25, 181, 21, 194, 253, 1, 11
   (a) **(4%)** For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with 16 one-word blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty. Please also calculate the overall miss rate accordingly.
   (b) You are asked to optimize a cache design for the given references. There are three possible direct-mapped cache designs, all with a total of 8 words of data: C1 has 1-word blocks, C2 as 2-word blocks, and C3 has 4-word blocks.
      I. **(3%)** In terms of miss rate, which cache design is the best?
      II. **(3%)** If the miss stall time is 25 cycles, and C1 has an access time of 2 cycles, C2 takes 3 cycles and C3 takes 5 cycles, which is the best cache design?
   (c) **(5%)** Show the final cache content for a three-way set associative cache with two-word blocks and a total size of 24 words. Use LRU replacement. For each reference, identify the index bits, the tag bits, the block offset bits and if it is a hit or a miss, assuming the cache is initially empty. Please also calculate the overall miss rate accordingly.
   (d) **(5%)** Show the final cache content for a fully associative cache with one-word blocks and a total size of 8 words. Use LRU replacement. For each reference, identify the index bits, the tag bits, the block offset bits and if it is a hit or a miss, assuming the cache is initially empty. Please also calculate the overall miss rate accordingly.

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5. **[20%]** Please design a finite-state machine based cache controller. The key characteristics of the target cache are shown below.
   - Direct-mapped cache
   - Write-back using write allocate
   - Block size is 4 words (16 bytes)
   - Cache size is 32 KB, so it holds 2048 blocks
   - 32-byte addresses
   - The cache includes a valid bit and a dirty bit per block

   The signals between the processor and the cache are.
   - 1-bit Read or Write signal
   - 1-bit Valid signal, saying whether there is a cache operation or not
   - 32-bit address
   - 32-bit data from processor to cache
   - 33-bit data from cache to processor
   - 1-bit Ready signal, saying the cache operation is complete

   (a) **(10%)** Please draw the state diagram of your designed finite-state machine based cache controller with all necessary signals in each state and transitions between states.
   (b) **(10%)** Explain in details the functionalities of each state and transitions between states.