國立中央大學111學年度碩士班考試入學試題

所別： 資工類　　共8頁 第1頁

科目： 作業系統與計算機組織

一、單選題　　（每題5分，答錯倒扣2分，倒扣至單選題0分為止）

1. We define the speedup of a system by the execution time before improvement divides the execution time after improvement. Suppose a module accounts for 40% computation time of the entire system. We enhance the module to be 10 times faster. What is the overall speedup after the enhancement (approximate to two decimal places)?
   a) 1.40
   b) 2.17
   c) 1.56
   d) 1.10
   e) None of the above

2. For a 16K-byte two-way set associative cache whose block size is 4 bytes, if the length of the address is 32 bits, how many bits are used for tag?
   a) 15
   b) 16
   c) 17
   d) 18
   e) 19

3. Assume that an un-pipelined machine has 8ns clock cycles. The machine uses four cycles for ALU operations, five cycles for branches, and five cycles for memory operations. The relative frequencies of these operations are 30%, 30%, and 40%, respectively. Suppose that pipelining the machines adds 1ns of overhead to the clock cycle time. Assume that the ideal CPI is one after pipelining. Ignore any other impact. What is the speedup in the instruction execution rate gained from pipelining the machine?
   a) 4.07
   b) 4.18
   c) 4.29
   d) 4.33
   e) 4.51

注意:背面有試題

4. Consider the C code on the right side. A user executes the executable of the code on a Linux shell. Assume it executed successfully. How many processes have been created by executing the C code, including the original process that executes main( )?
   a) 4
   b) 5
   c) 16
   d) 17
   e) 33

```
...
int main() {
  pid_t pid;
  int i=0;
  for (i=0;i<4;i++) {
    pid = fork();
    if (pid <0) {
      fprintf(stderr,"fork error\n");
      exit(-1);
    }
  }
  return 0;
}
```

5. Consider the CPU burst timeline of four processes, as shown on the right side. The processes need to share one CPU, and the OS uses the round-robin algorithm with time quantum = 5 for scheduling. Let the context switch time be very close to 0. Let the average waiting time of the processes be *t*. Which of the following is true?
   a) $6 \geqq t \geqq 5$
   b) $12 \geqq t \geqq 11$
   c) $11 \geqq t \geqq 10$
   d) $5 \geqq t \geqq 4$
   e) None of the above

Process	Arrival Time	Burst Time
P1	0	10
P2	1	6
P3	12	2
P4	13	3

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本科考試禁用計算器 ＊請在答案卷(卡)內作答

6. Memory page-replacement algorithms may have different page fault rates. Given the reference string "1 5 4 6 4 1 5 4 1 6 2 3 1 6"and the number of page frames 3, which of the following is true?
   a) The number of page faults is 8 when the FIFO algorithm is used.
   b) The number of page faults is 8 when the stack-based LRU algorithm is used.
   c) The number of page faults is 8 when the optimal algorithm is used
   d) The optimal algorithm has the best performance among all the page replacement algorithms, and thus modern OSes usually use this algorithm to implement memory page replacement.
   e) None of the above.

7. Which of the following is not true?
   a) Kubernetes, also known as K8s, is a system for automating deployment, scaling, and management of containerized applications.
   b) Docker is a system that virtualizes hardware.
   c) Para-virtualization is the technique in which the guest operating system is modified to work in cooperation with the VMM to optimize performance.
   d) Para-virtualization allows virtualization of older x86 CPUs (and others) without binary translation.
   e) Java virtual machine includes garbage collection to automatically reclaim memory (Java objects) no longer in use.

注意:背面有試題

8. The right side shows a solution to the producer-consumer problem with *n* buffers using three semaphores, where *empty=n*, *mutex=1*, and *full=0* at the initial state. Some variables are missing in the consumer program. What are they?
   a) V1=mutex, V2=empty
   b) V1=mutex, V2=full
   c) V1=empty, V2=mutex
   d) V1=full, V2=empty
   e) V1=full, V2=mutex

```
do {
   wait( V1 );
   wait( V2 );
      . . .
   // remove an item
      . . .
   signal( [    ] );
   signal( [    ] );
      . . .
   // consume the item
      . . .
}while (TRUE);
```

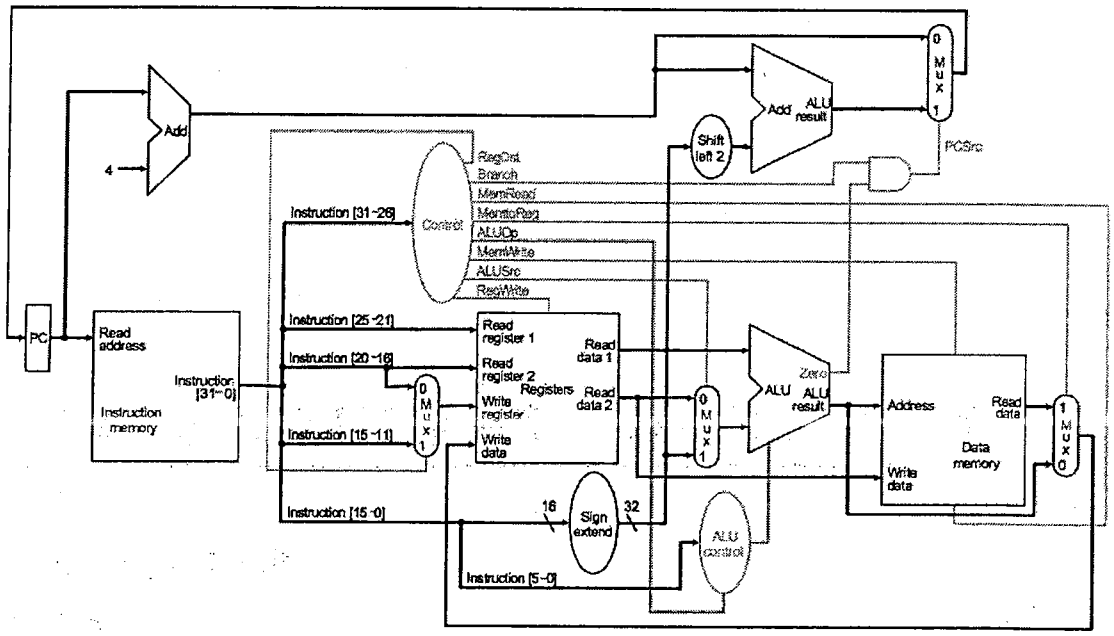
The structure of the consumer process.

```
do {
      . . .
   // produce an item in nextp
      . . .
   wait(empty);
   wait(mutex);
      . . .
   // add nextp to buffer
      . . .
   signal(mutex);
   signal(full);
}while (TRUE);
```

The structure of the producer process.

二、多選題（每題五分，每個選項單獨計分，答錯一個選項倒扣一分，倒扣至多選題0分為止）

9. The architecture of a single cycle CPU is shown in the following Figure. Select the correct statements based on the Figure.
   a) Sending the value of PC register to an adder can determine the register number for rd (the register destination operand).
   b) Performing "Sign extend" to the Instruction[15-0] produces an signed integer with 32 bits.
   c) Sending the Zero signal from the ALU to the AND gate determines whether Instruction[31-26] represents Branch operator or not.
   d) The Mux before the "Write register" determines whether to write new data to the destination register or not.
   e) None of the above.



10. The IEEE 754 standard specifies a binary16 as sign bit (1 bit), exponent (5 bits), and significand (10 bits). The exponent bias is 15. We define a new format by increasing the exponent to 8 bits and decreasing significand to 7 bits. We set the exponent bias in the new format as 127. which of the following statements are true?
    a) The new format has a larger dynamic range.
    b) The new format has a lower precision.
    c) Based on IEEE 754, a 16-digit binary number 0100 0010 0000 0000 represents the decimal number 3.
    d) Based on the new format, a 16-digit binary number 0100 0010 0000 0000 represents the decimal number 32.
    e) None of the above.

11. Which of the following statements are true regarding inclusive cache?
    a) The top-level cache is a subset of the bottom-level cache.
    b) If a block A is presented in both L1 and L2 cache where L2 is inclusive of L1, evicting the block A from L1 will cause L2 to evict block A.
    c) Inclusive cache utilizes the available cache space more efficiently.
    d) Inclusive cache ensures data consistency in the bottom-level cache.
    e) None of the above.

12. Which of the following statements are true regarding Instruction cache (I-cache) and Data cache (D-cache) in L1 cache?
    a) Compared with the original I-cached miss rate, the L1 cache miss rate will increase when I-cache and D-cache are merged.
    b) The L1 cache miss rate will decrease when I-cache and D-cache are merged, compared with the original D-cache miss rate.
    c) We can use different path to access instruction and data at the same time.
    d) Using separated I-cache and D-cache instead of a unified cache can reduce structural hazard.
    e) None of the above.

13. Which of the following statements are NOT true for instruction set design and CPU implementation?
    a) The advantages of dynamic scheduling include memory latency hiding and resolving real dependence which is unknown at compile time.
    b) For single-cycle implementation of CPU, the clock cycle is determined by the longest possible path.
    c) Compared to Memory-Memory architecture or Register-Memory architecture, Register-Register architecture has the advantage of having larger variation in Clock Cycle Per Instruction (CPI).
    d) Reduced Instruction Set Computer (RISC) has become mainstream products.
    e) Single-cycle implementation of CPU is more suitable for pipeline implementation compared with multi-cycle implementation.

14. Which of the following statements are true for pipeline hazards?
    a) Compliers can schedule the instructions to avoid some pipeline hazards.
    b) Using separated instruction cache and data cache instead of a unified cache could mainly reduce structural hazard.
    c) Write after read (WAR) hazards can be resolved by register renaming.
    d) Read after write (RAW) hazards can be resolved by register renaming.
    e) None of the above.

15. Which of the following statements are true?
    a) Increasing associativity of a cache would usually reduce the miss rate and the hit time.
    b) The branch offset field in the MIPS instruction is specified as a multiple of 4, i.e. a branch offset of 1 means 4 bytes. This enables a much larger range of branch offsets than if the offset were specified in bytes.
    c) We can always increase the hit rate by increasing the size of a cache.
    d) Pipeline registers between stages are necessary when performing pipelining.
    e) MIPS instructions are 32 bits.

16. Choose the correct statements from the multiple choices regarding contention scope
    a) Kernel thread scheduled onto available CPU is SCS.
    b) Linux allows only PTHREAD_SCOPE_PROCESS.
    c) Systems using the one-to-one model schedule threads using only SCS.
    d) In Pthread scheduling API, PTHREAD_SCOPE_SYSTEM schedules threads using PCS scheduling.
    e) None of the above

17. Choose the correct statements from the multiple choices regarding processor affinity
    a) Linux supports hard affinity only.
    b) Load balancing often counteracts the benefits of processor affinity.
    c) The main-memory architecture of a system can affect processor affinity.
    d) Soft affinity means that the process may require software that is available at only a particular site.
    e) None of the above

18. Choose the correct statements from the multiple choices regarding network protocols
    a) The BGP protocol is an intra-AS routing protocol.
    b) HTTP adopts TLS to encrypt messages.
    c) ARP requests are broadcast packets.
    d) The ARP spoofing attack is to associate IP addresses to the wrong MAC address.
    e) None of the above

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19. Choose the correct statements from the multiple choices
    a) Threads that are part of the same process share the same stack
    b) Threads that are part of the same process can access the same TLB entries.
    c) A process is trashing if it is spending more time executing than paging.
    d) Thrashing can be entirely solved by using a local replacement algorithm.
    e) None of the above

20. Choose the correct statements from the multiple choices
    a) Data access is one of reasons for process migration.
    b) The standard UNIX pipe mechanism allows process migration.
    c) Modularity is one of reasons for process cooperation.
    d) Shared memory is one of models for interprocess communications among cooperating processes.
    e) None of the above

注意:背面有試題