國立中山大學114學年度
碩士班考試入學招生考試試題

科目名稱：電子學(含數位電路)【IC設計領域聯招碩士班、電機系碩士班己組、IC設計所碩士班】

—作答注意事項—

考試時間：100分鐘

- **考試開始鈴響前不得翻閱試題，並不得書寫、劃記、作答。**請先檢查答案卷（卡）之應考證號碼、桌角號碼、應試科目是否正確，如有不同立即請監試人員處理。
- **答案卷限用藍、黑色筆(含鉛筆)書寫、繪圖或標示**，可攜帶橡皮擦、無色透明無文字墊板、尺規、修正液（帶）、手錶(未附計算器者)。每人每節限使用一份答案卷，請衡酌作答。
- 答案卡請以2B鉛筆劃記，不可使用修正液（帶）塗改，未使用2B鉛筆、劃記太輕或污損致光學閱讀機無法辨識答案者，後果由考生自負。
- 答案卷（卡）應保持清潔完整，不得折疊、破壞或塗改應考證號碼及條碼，亦不得書寫考生姓名、應考證號碼或與答案無關之任何文字或符號。
- 可否使用計算機請依試題資訊內標註為準，如「可以」使用，廠牌、功能不拘，唯不得攜帶書籍、紙張（應考證不得做計算紙書寫）、具有通訊、記憶、傳輸或收發等功能之相關電子產品或其他有礙試場安寧、考試公平之各類器材入場。
- **試題及答案卷（卡）請務必繳回，未繳回者該科成績以零分計算。**
- **試題採雙面列印，考生應注意試題頁數確實作答。**
- **違規者依本校招生考試試場規則及違規處理辦法處理。**

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※本科目依簡章規定「可以」使用計算機（廠牌、功能不拘）（問答申論題）

[Problem 1] (15%)

(a) What are the two main types of power consumption in CMOS circuits? Explain their sources and characteristics. (5%)

(b) How can we calculate these two power consumption types, respectively? Please list the equations together with the required parameters and their meanings (6%)

(c) How can we design a CMOS circuit to minimize these two types of power consumption? List and explain two strategies for each type of power consumption. (4%)

[Problem 2] (20%)

(a) Explain the role of PMOS and NMOS transistors in CMOS logic gates and why they are used in complementary pairs? (5%)

(b) Design a CMOS circuit for an XOR gate using the Boolean expression $Y = A\bar{B} + \bar{A}B$. Explain the implementation process. (10%)

(c) If each transistor introduces a delay of 1ns, estimate the total propagation delay of the circuit. (5%)

[Problem 3] (15%)

(a) What is propagation delay in CMOS logic gates and why is it a critical parameter in digital circuit design? (3%)

(b) Explain the two types of propagation delay and their difference (4%) Why are these values often different? (2%)

(c) What is noise margin in CMOS logic circuits, and why is it important for reliable operation? (2%)

(d) Define Noise Margin High (*NMH*) and Noise Margin Low (*NML*) for CMOS logic gates and how they are calculated. Please also explain each parameter you used. (4%)

[Problem 4] (20%)

(a) Sketch the circuit diagram of the basic CMOS inverter. (5%)

(b) Plot the $V_o - V_i$ VTC (Voltage-Transfer Characteristic) curve of the CMOS inverter and divide the VTC curve into several portions according to the operating region of the transistors. (Assume that the transistors are matched.) (5%)

(c) Indicate the boundary conditions between each portion in the VTC curve. (5%)

(d) Sketch the current in the CMOS inverter versus the input voltage and indicate the boundary conditions and the peak current. (5%)

[Problem 5] (30%)

(a) Determine the logic function at the output Y of the following circuit in Fig. 1. Notably, C_{L1} and C_{L2} represent the overall parasitic capacitance at node M and N, respectively. (5%)

(b) What is the name of the circuit with a similar structure to the following circuit. (3%)

(c) Explain the operation of the circuit in Fig. 1 with respect to the logic state of the signal ϕ_1 and ϕ_2. (5%)

(d) Assume that the circuit is fabricated in a 0.18-μm CMOS technology for which VDD = 1.8 V, $V_{tn} = |V_{tp}| = 0.5$ V and $\mu_n C_{ox} = 3\mu_p C_{ox} = 300\ \mu A/V^2$. The W/L ratios of PMOS and NMOS devices are with 0.54 μm/0.18 μm and 0.27 μm/0.18 μm, respectively. C_{L1} and C_{L2} are found to be 50 fF. Estimate the rising time (t_r) of the signal at node N. (5%)

(e) Follow Problem 5 (d) and estimate the falling time (t_f) of the signal at node N, assuming that the gate drive voltages of $M_{N4} \sim M_{N7}$ are at logic 1, simultaneously. (7%)

(f) Describe the major problem in the circuit of Fig. 1. (5%)

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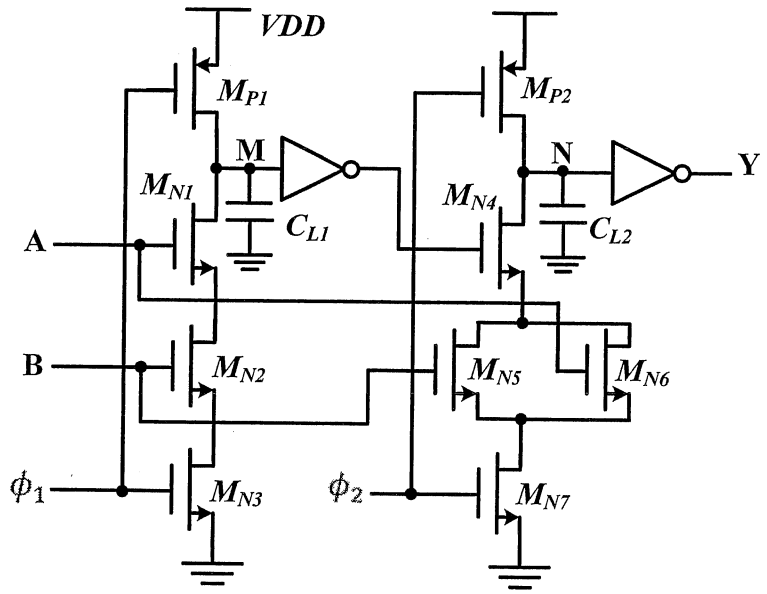

Fig. 1 The circuit diagram for Problem 5.