# 國立中正大學
# 114學年度碩士班招生考試
# 試 題

[第3節]

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|---|---|
| 科目名稱 | 計算機組織 |
| 系所組別 | 電機工程學系－ 計算機工程組<br>晶片系統組 |

**－作答注意事項－**

※作答前請先核對「試題」、「試卷」與「准考證」之系所組別、科目名稱是否相符。

1. 預備鈴響時即可入場，但至考試開始鈴響前，不得翻閱試題，並不得書寫、畫記、作答。
2. 考試開始鈴響時，即可開始作答；考試結束鈴響畢，應即停止作答。
3. 入場後於考試開始40分鐘內不得離場。
4. 全部答題均須在試卷（答案卷）作答區內完成。
5. 試卷作答限用藍色或黑色筆（含鉛筆）書寫。
6. 試題須隨試卷繳還。

# 國立中正大學 114 學年度碩士班招生考試試題

科目名稱：計算機組織　　本科目共 2 頁　第 1 頁

系所組別：電機工程學系-計算機工程組、晶片系統組

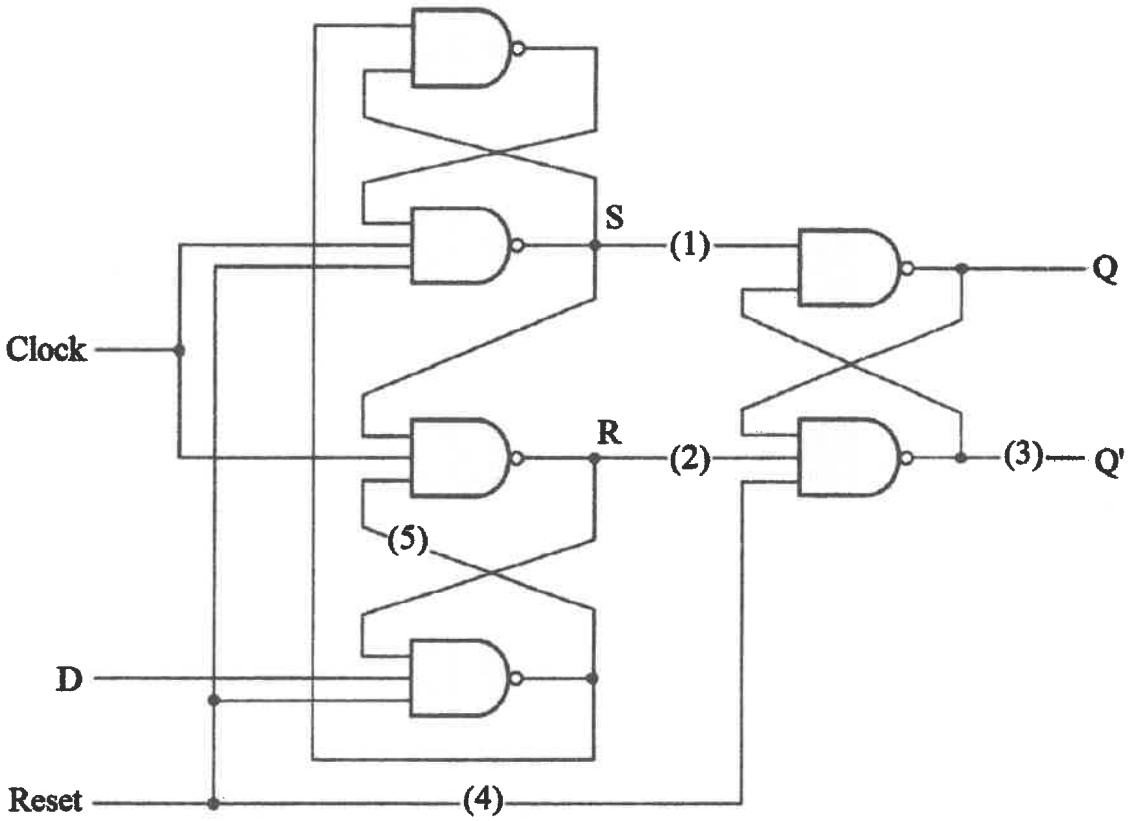
1. (20%) Assume the MIPS CPU's register is designed as in the diagram below. Please write down the data at (1), (2), (3), (4), and (5) with the conditions for:

   (a) (5%) Normal condition D= 0, Clock= 1 steady, then changes to D= 1, Clock= 0.

   (b) (5%) Normal condition D= 1, Clock= 1 steady, then changes to D= 0, Clock= 1.

   (c) (5%) D= 1, Clock= 1 steady, then reset the register.

   (d) (5%) (Q, Q') = (1, 1) in the beginning, next D= 0, Clock = 1 steady.




2. (20%) Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2. Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D.

   (a) (10%) What is the global CPI for each implementation?

   (b) (10%) Find the clock cycles required in both cases.

3.(20%) Consider the following MIPS loop as:

```
LOOP:  slt $t2, $0, $t1
       beq $t2, $0, DONE
       subi $t1, $t1, 1
       addi $s2, $s2, 2
       j LOOP
DONE:
```

(a). (10%) Assume that the register **$t1** is initialized to the value 10. What is the value in register **$s2** assuming the **$s2** is initially zero?

(b). (10%) For each of the loops above, write the equivalent C code routine. Assume that the registers **$s2**, **$t1**, and **$t2** are integers **B**, **i**, and **temp**, respectively.

4. (20%) Please calculate follows in binary and then represent in IEEE 754 single precision binary formats:

(a). (10%) -0.4375×0.75, (b). (10%) 2.75 / 0.125.

5. (20%) we assume that the following MIPS code is executed on a pipelined processor with a 5-stage pipeline, full forwarding, and a predict-taken branch predictor:

```
        lw r2, 0(r1)
label1: beq r2, r0, label2 # not taken once, then taken
        lw r3, 0(r2)
        beq r3, r0, label1 # taken
        and r1, r3, r1
label2: sw r1, 0(r2)
```

(a). (10%) Draw the pipeline execution diagram for this code, assuming there are no delay slots and that branches execute in the EX stage.

(b). (10%) Repeat question (a), but assume that delay slots are used. In the given code, the instruction that follows the branch is now the delay slot instruction for that branch.