國立中山大學114學年度
碩士班考試入學招生考試試題

科目名稱：電子學(甲組)【電機系碩士班甲組】

—作答注意事項—

考試時間：100分鐘

- **考試開始鈴響前不得翻閱試題，並不得書寫、劃記、作答。**請先檢查答案卷（卡）之應考證號碼、桌角號碼、應試科目是否正確，如有不同立即請監試人員處理。
- **答案卷限用藍、黑色筆(含鉛筆)書寫、繪圖或標示**，可攜帶橡皮擦、無色透明無文字墊板、尺規、修正液（帶）、手錶(未附計算器者)。每人每節限使用一份答案卷，請衡酌作答。
- 答案卡請以2B鉛筆劃記，不可使用修正液（帶）塗改，未使用2B鉛筆、劃記太輕或污損致光學閱讀機無法辨識答案者，後果由考生自負。
- 答案卷（卡）應保持清潔完整，不得折疊、破壞或塗改應考證號碼及條碼，亦不得書寫考生姓名、應考證號碼或與答案無關之任何文字或符號。
- 可否使用計算機請依試題資訊內標註為準，如「可以」使用，廠牌、功能不拘，唯不得攜帶書籍、紙張（應考證不得做計算紙書寫）、具有通訊、記憶、傳輸或收發等功能之相關電子產品或其他有礙試場安寧、考試公平之各類器材入場。
- **試題及答案卷（卡）請務必繳回，未繳回者該科成績以零分計算。**
- **試題採雙面列印，考生應注意試題頁數確實作答。**
- **違規者依本校招生考試試場規則及違規處理辦法處理。**

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科目名稱：電子學(甲組)【電機系碩士班甲組】　　題號：431006

※本科目依簡章規定「可以」使用計算機（廠牌、功能不拘）(問答申論題)　共 2 頁第 1 頁

1. (30%) It is required to use a peak rectifier to design a dc power supply that provides an average dc output voltage of 12 V on which a maximum of ±1-V ripple is allowed. The rectifier feeds a load of 200 Ω. The rectifier is fed from the line voltage (120 V rms, 60 Hz) through a transformer. The diodes available have 0.7-V drop when conducting. If the designer opts for the full-wave bridge-rectifier circuit:
   (a) (10%) Specify the rms voltage that must appear across the transformer secondary.
   (b) (10%) Find the required value of the filter capacitor.
   (c) (10%) Find the maximum reverse voltage that will appear across the diode, and specify the PIV rating of the diode.

2. (20%) A series-shunt feedback amplifier is shown in **Figure 1.** All three MOSFETs are biased to operate at g_m= 4 mS. You can neglect their channel length modulation effect.
   (a) (10%) Select a value for R_F that results in a closed-loop gain that is ideally 10 V/V
   (b) (10%) How can you adjust the circuit to make A_f equal to 10?

3. (25%) In the common-gate amplifier circuit of **Figure 2**, Q_2 and Q_3 are matched. $k_n'(W/L)_n = k_p'(W/L)_p = 4$ mA/V^2, and all transistors have $|V_t| = 0.8$ V and $|V_A| = 20$ V. The signal v_{sig} is a small sinusoidal signal with no dc component.
   (a) (5%) Neglecting the effect of V_A, find the required value of V_{BIAS}. (For DC analysis, $v_{sig} = 0$ V)
   (b) (10%) Find the values of R_{in} and R_{out}.
   (c) (5%) Calculate the voltage gain v_o/v_{sig}.
   (d) (5%) How large can v_{sig} (amplitude) be while maintaining saturation-mode operation for Q_1 & Q_2?

4. (25%) **Figure 3** shows a three-stage amplifier in which the stages are directly coupled. The bypass capacitors are large enough to act as perfect short circuits at all signal frequencies of interest. Thermal voltage is 25 mV.
   (a) (10%) Find the dc bias emitter current in Q_2 and Q_3. Assume V_{BE} = 0.7 V, β = 100, and neglect the Early effect.
   (b) (10%) Find the input resistance and the output resistance.
   (c) (5%) Calculate the voltage gain v_o/v_i.

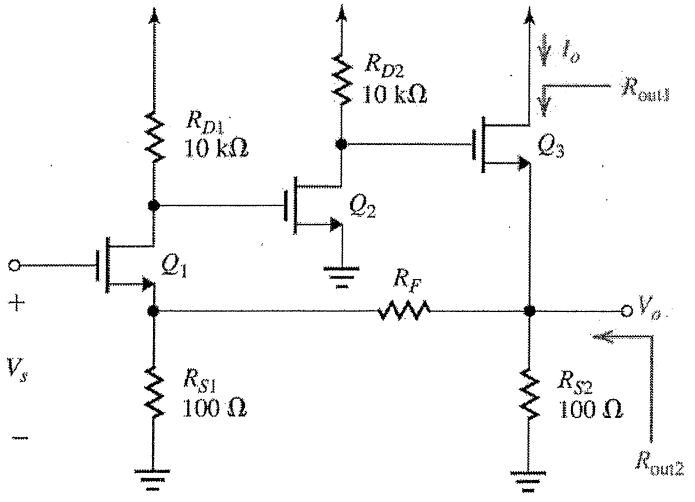

Figure 1

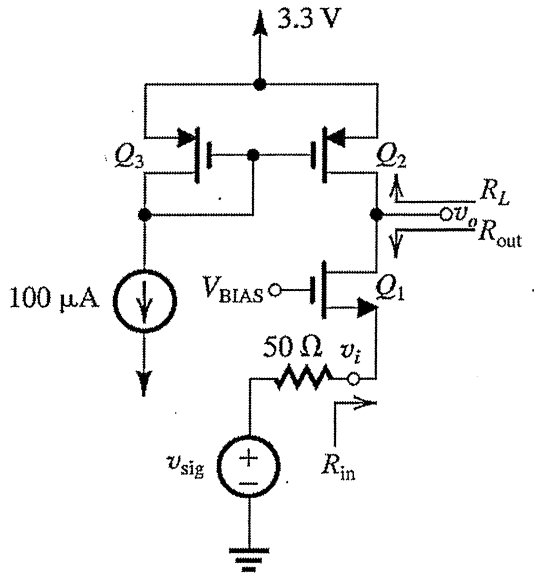

Figure 2

試題請隨卷繳回，請留意背面是否有題

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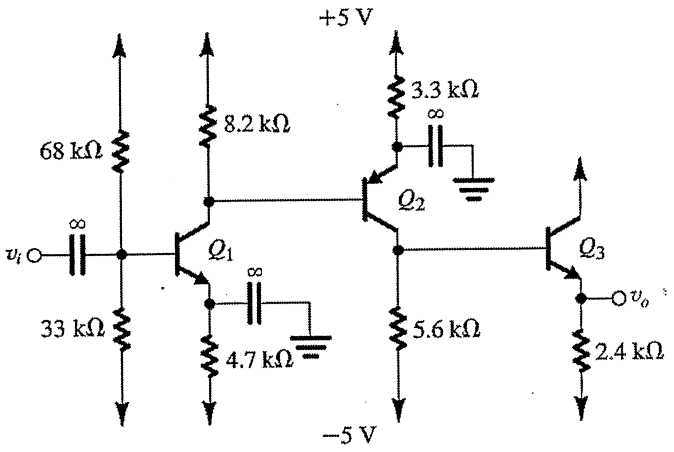

Figure 3