國立中山大學113學年度
碩士班暨碩士在職專班招生考試試題

科目名稱：數位系統設計【IC設計所碩士班】

—作答注意事項—

考試時間：100分鐘

- **考試開始鈴響前不得翻閱試題，並不得書寫、劃記、作答。**請先檢查答案卷（卡）之應考證號碼、桌角號碼、應試科目是否正確，如有不同立即請監試人員處理。
- **答案卷限用藍、黑色筆(含鉛筆)書寫、繪圖或標示**，可攜帶橡皮擦、無色透明無文字墊板、尺規、修正液（帶）、手錶(未附計算器者)。每人每節限使用一份答案卷，請衡酌作答。
- 答案卡請以2B鉛筆劃記，不可使用修正液（帶）塗改，未使用2B鉛筆、劃記太輕或污損致光學閱讀機無法辨識答案者，後果由考生自負。
- 答案卷（卡）應保持清潔完整，不得折疊、破壞或塗改應考證號碼及條碼，亦不得書寫考生姓名、應考證號碼或與答案無關之任何文字或符號。
- 可否使用計算機請依試題資訊內標註為準，如「可以」使用，廠牌、功能不拘，唯不得攜帶書籍、紙張（應考證不得做計算紙書寫）、具有通訊、記憶、傳輸或收發等功能之相關電子產品或其他有礙試場安寧、考試公平之各類器材入場。
- 試題及答案卷（卡）請務必繳回，未繳回者該科成績以零分計算。
- 試題採雙面列印，考生應注意試題頁數確實作答。
- 違規者依本校招生考試試場規則及違規處理辦法處理。

國立中山大學113學年度碩士班暨碩士在職專班招生考試試題

科目名稱：數位系統設計【IC設計所碩士班】　　題號：483001

※本科目依簡章規定「可以」使用計算機（廠牌、功能不拘）（問答申論題）　　共2頁第1頁

[Problem 1] **(20%)** Implement the following Boolean function

$F(w, x, y, z) = xy + w'x'z' + wx'y'z' + wx'yz.$

(a) by using only NOR gates. (5%)
(b) by using only NAND gates. (5%)
(c) by using the simplest sum-of-products form (5%)
(d) by drawing the logic diagram using a multiplexer (5%)

Please note that for (a), (b) and (c) you need to show the final Boolean function and how you derive the function.

[Problem 2] **(12%)** Short answer questions:

(a) Provide an example to demonstrate that a Boolean function can have more than one simplest form of expression, indicating its non-uniqueness. (3%)
(b) Provide an overview of the hardware structure of a sequential circuit and utilize this structure to explain how a sequential circuit is different in functionality and design from a combinational circuit. (4%)
(c) Present several waveform diagrams to illustrate and clarify the concepts of setup time and hold time in a D flip-flop. (5%)

[Problem 3] **(18%)** Design an asynchronously resettable positive edge-triggered finite state machine that accepts a one-bit input d and generates two one-bit outputs x and y. x should be 1 if d has been 0 for at least two consecutive cycles. y should be 1 if d has been 0 for at least three cycles (not necessarily consecutively).

(a) Give Verilog/VHDL codes of an asynchronously resettable positive edge-triggered flip-flop. (3%)
(b) Draw the state transition diagram and define each state clearly. (5%)
(c) Write RTL Verilog/VHDL codes to implement the finite state machine you designed in (b). (10%)

[Problem 4] **(20%)** (a) Assume that the 4-bit binary adders are available. Please design a combinational circuit for the addition of two BCD digits using the 4-bit binary adder. Please draw the final logic circuit of the BCD adder with the 4-bit binary adder circuit block. Please note that you don't have to show the details of the 4-bit binary adder. (10%) (b) Design a combinational circuit that generates the 9's complement of a BCD digit. Please note that you need to show the final Boolean function and how you derive the function. (10%)

[Problem 5] **(15%)** (a) Design a counter with T flip-flops that goes through the following binary repeated sequence: 0, 1, 3, 7, 6, 4. Show that when binary states 010 and 101 are considered as don't care conditions, the counter may not operate properly.(10%) (b) Find a way to correct the design. (5%) Please note that you need to show the final Boolean function, the state diagram and how you derive the function.

[Problem 6] **(15%)** A circuit for a gated D-latch is shown in Fig. 1. Assume that the propagation delay through a NAND gate or an inverter is 1 ns. Complete the timing diagram given in the Fig. 2, which shows the signal values with 1 ns resolution. Please note that you need to redraw the timing diagram in your answer sheet.

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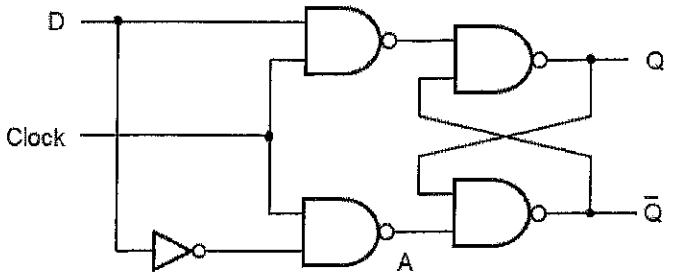

Fig. 1

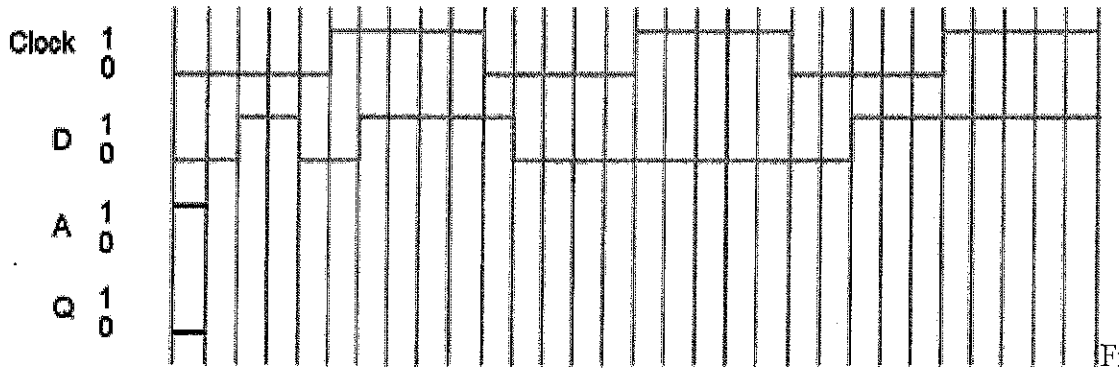

Fig. 2