

國立中正大學

112 學年度碩士班招生考試

試題

[第 2 節]

科目名稱	電子學
系所組別	機械工程學系光機電整合工程

—作答注意事項—

※作答前請先核對「試題」、「試卷」與「准考證」之系所組別、科目名稱是否相符。

1. 預備鈴響時即可入場，但至考試開始鈴響前，不得翻閱試題，並不得書寫、畫記、作答。
2. 考試開始鈴響時，即可開始作答；考試結束鈴響畢，應即停止作答。
3. 入場後於考試開始 40 分鐘內不得離場。
4. 全部答題均須在試卷（答案卷）作答區內完成。
5. 試卷作答限用藍色或黑色筆（含鉛筆）書寫。
6. 試題須隨試卷繳還。

國立中正大學 112 學年度碩士班招生考試試題

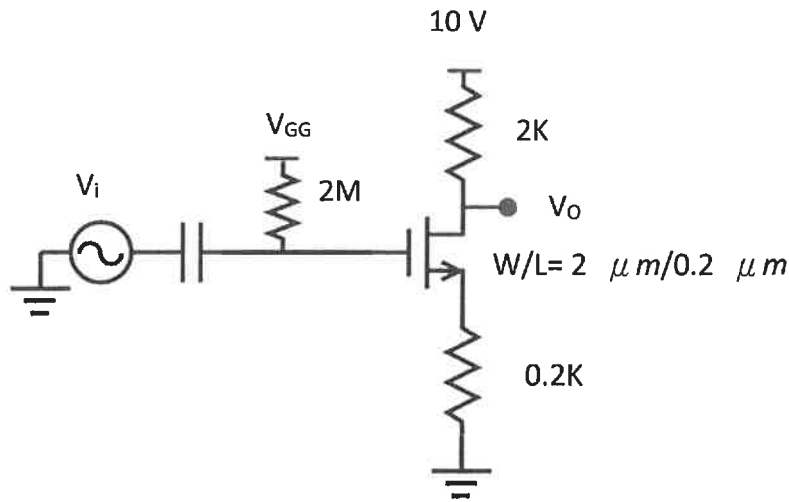
科目名稱：電子學

本科目共 2 頁 第 1 頁

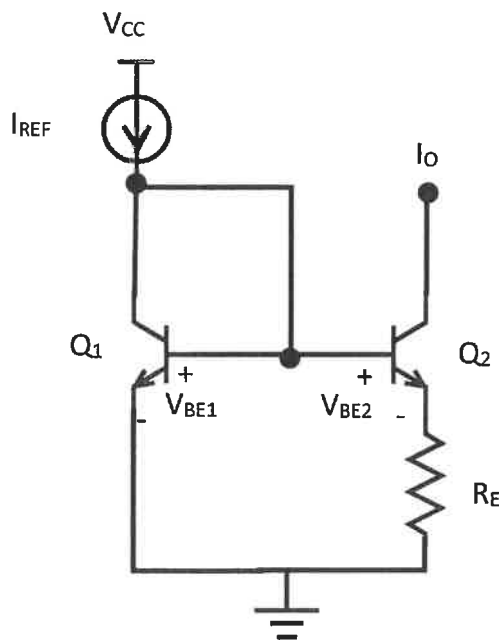
系所組別：機械工程學系光機電整合工程

1. (25%) For circuit below, where V_{tn} (threshold voltage for NMOS) = $|V_{tp}|$ (threshold voltage for PMOS) = 1 V, $\mu_n C_{ox} = 2 \mu_p C_{ox} = 200 \mu A/V^2$ (C_{ox} is the oxide capacitance, μ_n is the mobility of the electrons, and μ_p is the mobility of the holes), $V'_A = 40 V/\mu m$ (V'_A is entirely process-technology dependent, as early voltage $V_A = V'_A L$).

Let drain current $I_D = 2 \text{ mA}$ is desired, please find (a) (5%) V_{GG} (circuit below), (b) (5%) g_m (transconductance), (c) (5%) r_o (output resistance due to the Early effect), (d) (5%) R_O (output resistance), (e) (5%) A_v (voltage gain).



2. (25%) For circuit below, where thermal voltage $V_T = 25 \text{ mV}$, $I_{REF} = 100 \mu A$, $I_O = 20 \mu A$, transistor parameters in current are $I_{S1} = I_{S2} = 5^{-15} \text{ A}$, please find (a) (5%) V_{BE1} , (b) (10%) V_{BE2} , (c) (10%) R_E



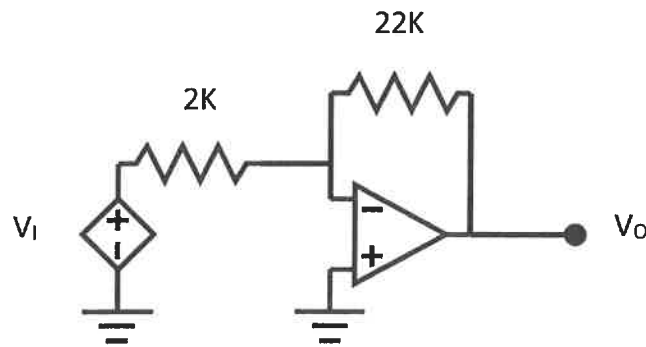
國立中正大學 112 學年度碩士班招生考試試題

科目名稱：電子學

本科目共 2 頁 第 2 頁

系所組別：機械工程學系光機電整合工程

3. (25%) For circuit below, please find voltage gain A_v .



4. (25%) Consider the Hybrid π model for BJT, where voltage across the base-emitter junction $V_{BE} = 0.9$ V, transistor parameter $\beta_0 = 100$, thermal voltage $V_T = 25$ mV, voltage across the collector-emitter junction $V_{CE} = 0.4$ V, early voltage $V_A = 40$ V. Let quiescent collector current $I_C = 4$ mA, please find (a) (5%) transconductance g_m , (b) (5%) base resistance (r_π), (c) (5%) transresistance (r_m), (d) (5%) output resistance (r_o), and (e) (5%) output conductance (g_{CE}).