元智大學 103 學年度研究所 碩士班 招生試題卷

系(所)別：電機工程學系碩士班　組別：不分組　科目：電子學　用紙第 1 頁共 2 頁

●不可使用電子計算機

1. (15%) For the circuit shown in Fig. 1, assume $\lambda \neq 0$, V_b is DC bias voltage and transconductances of transistors M_1 and M_2 are g_{m1} and g_{m2}, respectively. Please derive (a) input impedance (5%), (b) output impedance (5%), and (c) voltage gain of this circuit (5%).

2. (15%) For the circuit shown in Fig. 2, assume $\lambda \neq 0$, V_b is DC bias voltage and transconductances of transistors M_1 and M_2 are g_{m1} and g_{m2}, respectively. Please derive (a) input impedance (5%), (b) output impedance (5%), and (c) voltage gain of this circuit (5%).

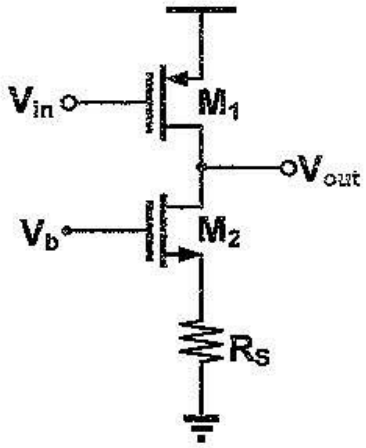

Fig. 1

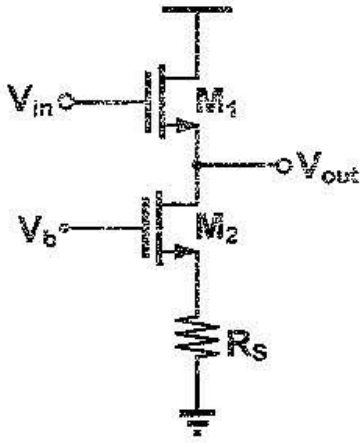

Fig. 2

3. (35%) The amplifier with feedback network is shown in Fig.3. If $\lambda \neq 0$ and transconductances for the NMOS transistors and PMOS transistors are g_{mN} and g_{mP}, please derive

[Note: $R_1 + R_2$ is very large and $r_{o1} = r_{o2} = r_{oN}$, $r_{o3} = r_{o4} = r_{oP}$]

(a) What kind of feedback topology is it? (5%)
(b) Please derive the open-loop voltage gain? (10%)
(c) Please derive the open-loop output impedance? (5%)
(d) Please derive the closed-loop voltage gain? (10%)
(e) Please derive the closed-loop output impedance? (5%)

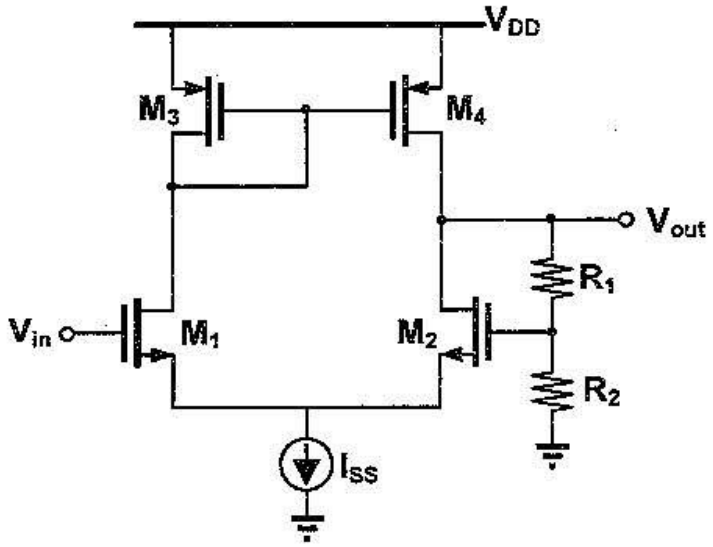

Fig. 3

4. (20%) (a) Please derive the truth table of a set/rest (SR) flip-flop. (5%) (b) Please draw a gate-level diagram of the SR flip-flop. (5%) (c) Please draw the complementary metal-oxide-semiconductor (CMOS) implementation of a clocked SR flip-flop. (5%) (d) Please sketch a rough layout of the CMOS implementation of the clocked SR flip-flop. (5%)

5. (15%) (a) Please describe the crosstalk effect between adjacent signal lines in a digital CMOS implementation. (7%) (b) Please describe the leakage power of a MOS circuit. (8%)