編號： 201

國立成功大學 109 學年度碩士班招生考試試題

系　　所：電機資訊學院-微電、奈米聯招

考試科目：固態電子元件

考試日期：0210，節次：2

※ 考生請注意：本試題可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. The electron concentration in a semiconductor at room temperature is given by $n(x) = 10^{18}\exp(-5x/L)\ \text{cm}^{-3}$，where $0 \le x \le L$ and $L = 2\times10^{-3}$ cm. Determine the electric field at $x = 0$ and the electron diffusion current at $x = L/2$ under thermal equilibrium, assume the electron mobility is $1500\ \text{cm}^2/\text{V}\cdot\text{s}$ and $kT/q = 26$ mV. (10%)

2. Please plot the possible potential distribution of an M/Si(p)/M structure, assume $\phi_m < \phi_{\text{Si}}$, where ϕ_m and ϕ_{Si} are the work function of the metal M and the p type silicon, respectively. (10%)

3. For the pn junction shown in Fig. 1, assume the doping concentration of the p and n type semiconductor are N_A and N_D, respectively. Please find the ratio of V_a/V_b and derive x_p as a function of V_a. (10%)

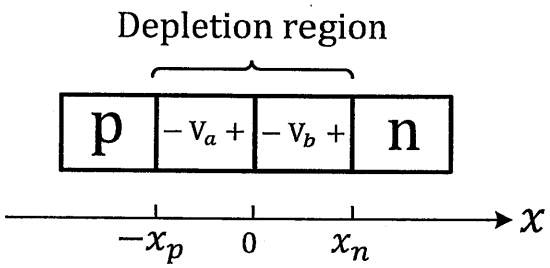

Fig. 1

4. If the energy band gap of the semiconductor (E_g) for a pn junction is reduced to be of $E_g/2$, please plot and explain how the diode current-voltage (I-V) characteristics will change. (10%)

5. Please use energy band diagram to explain the electric field effect of a MOS (p-Si) structure under strong inversion. Briefly describe the source of electrons in the inversion region. (10%)

6. Fig. 2 shows the typical common-emitter current gain, β_F as a function of collector current.

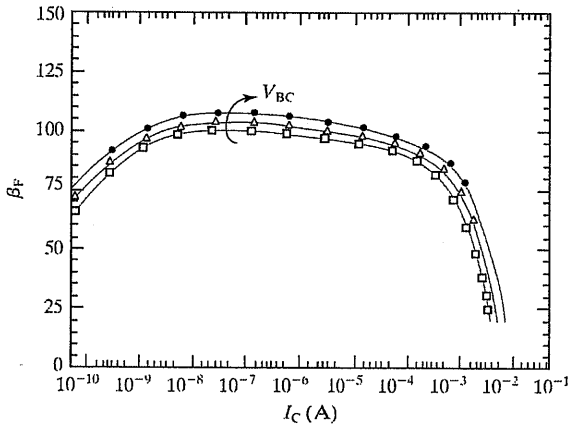

Fig. 2

Explain why β_F drops (a) when I_C is smaller than 10^{-8}A, and (b) when I_C is larger than 10^{-3}A. (10%)

7. In a heavily velocity-saturated n-MOSFET device, the velocity at the source end of the channel is already approximately v_{sat}. The inversion charge density per unit area at the source end is given by $Q_{inv} = - C_{ox}(V_{gs} - V_t)$. The transistor width is W. Derive an expression for the drain current I_d.(10%)

8. Calculate threshold voltage shift (ΔV_t) in an n-MOSFET due to fixed negative sheet charge at the SiO_2/Si interface (gate dielectric/channel interface) with density $10^{11}cm^{-3}$. The transistor has a high-K gate dielectric with relative dielectric constant ε_r=15.6 and thickness of 2.5nm. (10%)

9. Fig. 3 shows a typical I_d-V_{ds} characteristics of an n-MOSFET. Sketch a new I_d-V_{ds} curve to illustrate how this curve would change in the presence of drain-induced barrier lowering (DIBL) effect. (10%)

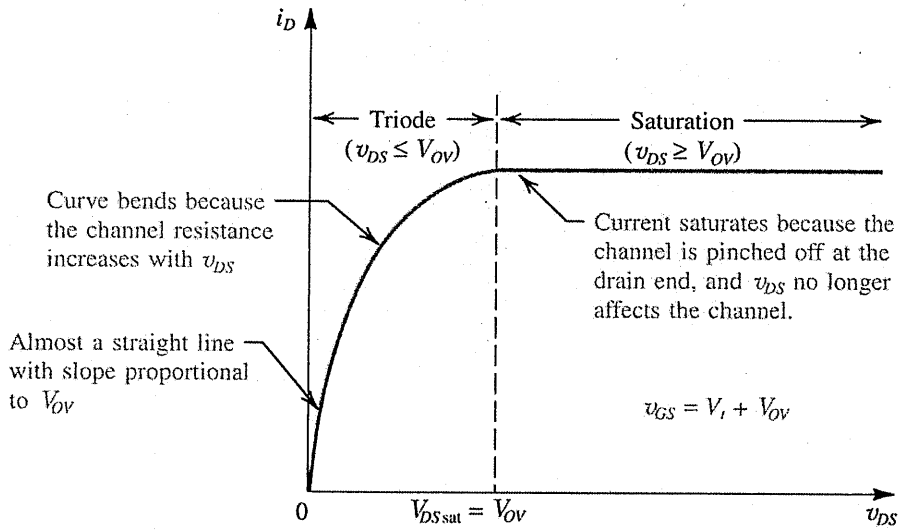

Fig. 3 (Sedra & Smith, 7th Ed.)

10. Which of the following statements is **FALSE** about n-MOS C-V characteristics (single-choice)? (5%)
    A. Quantum mechanical effects causes MOS inversion capacitance to increase.
    B. Poly-silicon depletion effects causes MOS inversion capacitance to decrease.
    C. Thicker gate dielectric causes the n-MOS threshold voltage to increase.
    D. Heavier body doping causes the n-MOS threshold voltage to increase
    E. Lower metal-gate work function causes the MOS flat-band voltage to decrease

11. Which of the following statements is **FALSE** about MOS leakage current and short channel effects? (single-choice) (5%)
    A. Typically, sub-threshold slope (SS) increases when gate length (L) decreases.
    B. Typically, nMOS threshold voltage increases when gate length (L) decreases.
    C. Gate leakage current is present when the gate dielectric is too thin.
    D. Gate-induced drain leakage (GIDL) flows from the drain to the body (substrate).
    E. Punch-through leakage current can be suppressed by increasing body doping concentration.