國立中正大學
109學年度碩士班招生考試
試 題

[第1節]

科目名稱	計算機組織
系所組別	電機工程學系－ 信號與媒體通訊組 計算機工程組 晶片系統組

－作答注意事項－

※作答前請先核對「試題」、「試卷」與「准考證」之系所組別、科目名稱是否相符。

1. 預備鈴響時即可入場，但至考試開始鈴響前，不得翻閱試題，並不得書寫、畫記、作答。
2. 考試開始鈴響時，即可開始作答；考試結束鈴響畢，應即停止作答。
3. 入場後於考試開始40分鐘內不得離場。
4. 全部答題均須在試卷（答案卷）作答區內完成。
5. 試卷作答限用藍色或黑色筆（含鉛筆）書寫。
6. 試題須隨試卷繳還。

國立中正大學 109 學年度碩士班招生考試試題

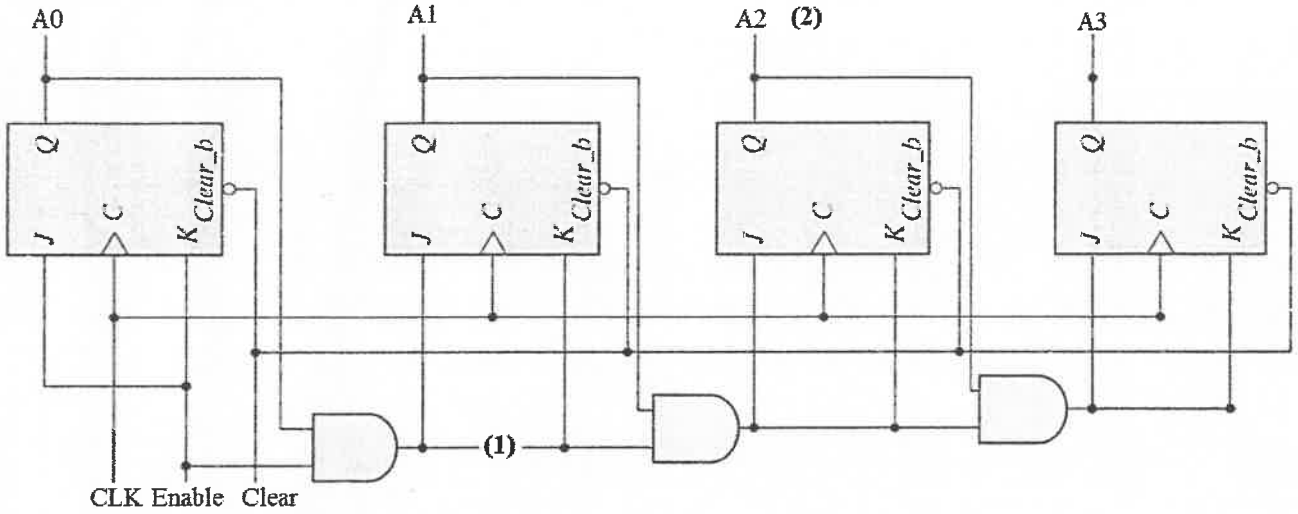
科目名稱：計算機組織　　本科目共 2 頁　第 1 頁

系所組別：電機工程學系-信號與媒體通訊組、計算機工程組、晶片系統組

1. (20%) Please tell the difference of:

   (a). Pipelining & Parallelism processing, (b). Latches & Flip-flops, (c). Wafers & Dies, (d). CPI & CPU time

2. (20%) A state generator in CPU controller which is synthesized as the circuit below. If the initial value of A0-A3 are all 0, please plot the timing sequence for the first five clocks with signals CLK, Enable, Clear, **(1)**, and **(2)** in diagram.



3. (20%) If a single-cycle CPU is designed with instructions of beq, sub, sd, and ld, please fill out asserted, de-asserted, and don't care signals by Table 1.

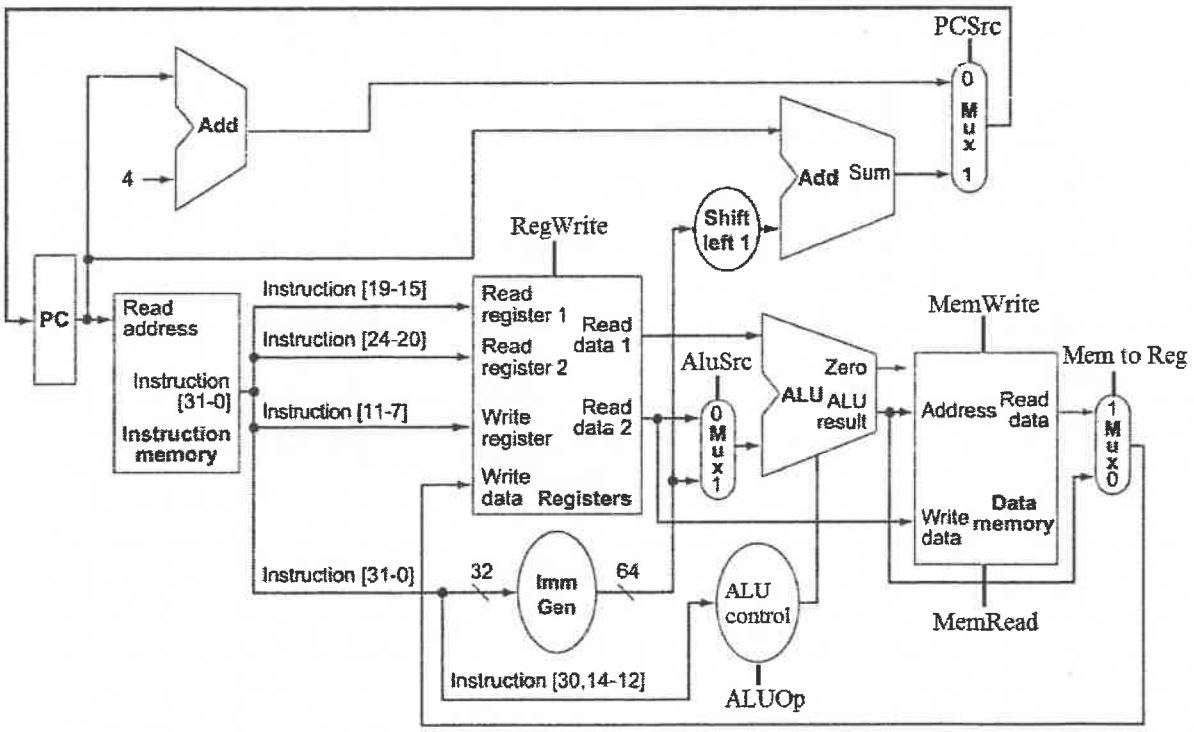


Table 1

Instruction	AluSrc	Mem to Reg	RegWrite	MemRead	MemWrite	PCSrc

4. (20%) Consider three CPUs P1, P2, P3 as below running with a same program, which is designed with 1.2×10^6 instruction A, 2.2×10^6 instruction B, and 0.5×10^6 instruction C:

	P1	P2	P3
Clock rates (GHz)	2	1	1.5
Average CPI	3	1.5	2

(a). (10%) Which processor has the highest performance in execution time?

(b). (10%) If we are going to increase the slowest CPU's speed in question (a) for 5% but lead to an increase of 12% in the CPI, what clock rate should be for this CPU?

5. (10%) Assume a 64-bit C codes with translated assembly codes as:

```
int i;
for (i = 0; i < 100; i++) {
result += MemArray[i];
}
return result;
```

```
        addi  x6, x0, 0
        addi  x29, x0, ?
Loop:   ld    x7, 0(x10)
        add   x5, x5, ?
        addi  x10, x10, ?
        addi  x6, x6, 1
        blt   ?, x29, ?
```

Please finish the assembly code by filling out the " ? " marks.

6. (10%) A cache holds 2048 doubleword:

(a). (5%) How many Tag bits are provided in a direct mapped 64-bit cache address?

(b). (5%) What is the total number of bits in such a cache?